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SCALING AND NUMERICAL SIMULATION ANALYSIS OF 50nm MOSFET INCORPORATING DIELECTRIC POCKET (DP-MOSFET)

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ABSTRACT

Characterization of a metal-oxide-semiconductor field effect transistor (MOSFET) incorporating dielectric pocket (DP) for suppression of short-channel effect (SCE) was demonstrated by using numerical simulation. The DP was incorporated between the channel and source/drain of planar MOSFET and was scaled to get an optimized structure. An analysis of current-voltage (I-V) of 50 nm channel length (Lg) has been done successfully. The DP has suppressed short channel effect (SCE) without the needs of decreasing the junction depth. A reduction of leakage current (IOFF) was obtained in MOSFET with DP without altering the drive current (ION). A very low leakage current is obtained for DP device with drain voltage (VDS) of 0.1 V and increase when VDS =1.0 V. Consequently, the threshold voltage (VT) is increased accordingly with the increasing of body doping. A better control of VT roll-off was also demonstrated better for MOSFET with DP as compared to conventional MOSFET. Thus, the incorporation of DP will enhance the electrical performance and give a very good control of the SCE for scaling the MOSFET in nanometer regime for future development of nanoelectronics product.

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