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STEREOMETRY OF VOIDS IN SOLDER INTERCONNECT BETWEEN PCB AND PACKAGING

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ABSTRACT

Metallurgical interconnecting between lead packages and Printed Circuit Board (PCB) was investigated focus on their microstructure which believed that can reveal the problem of solder interconnect failure in semiconductor packaging. Voids in a solder joint can reduce their fatigue life. Voids are caused by the presence of flux in solder paste during reflow soldering, and they are difficult to remove completely. We investigated void propagation in the solder interconnect joints of a semiconductor packaging and believe can be lead to a new crack propagation. Stereometry of voids and morphology of the joint was examined by using 3-D Stereology Microscope (IFM)® . 3D analysis of microstructure was carried out to obtain depth profile formation of voids streometry. The average of depth of 50 µm – 60 µm meanwhile diameter of 45 µm – 85 µm were observed. SEM analysis was also carried out to support all the data's obtained. These voids are believed to be linked with the formation of crack. Voids were found in the solder area for most of the samples studied.

http://journal.masshp.net/wp-content/uploads/Journal/2008/Jilid%202/A.%20Jalar%201-7.pdf

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