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# STENCIL PRINTING TECHNIQUE FOR MICRO-SOLDER BUMPS PATTERNING

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## ABSTRACT

Advancement in integrated circuit (IC) chips packaging involves three-dimensional (3D) versus two-dimensional (2D) packaging technology. 3D packaging involves stacking of daughter die/s on to a mother die in a vertical configuration for obvious reasons. Interconnections had been done either through wire bonding or a combination of wire bonding and flip chip technology. Flip chip technology requires the formation of solder bumps on processed silicon wafers, which were diced to form a single diced die. Relatively expensive and elaborate evaporation and electroplating processes used in the formation of solder bumps leads to a development in a simpler and cheaper bumping technology. The present experimental work describes challenges and updates methods in stencil printing for the development of solder bumps on copper as an arbitrary substrate. Both, lead-containing and lead-free solder pastes were used as the bumping materials of construction. Green solder bumps were heated in an atmospheric furnace with controlled heating rate and heating time. Solder pastes characterisation used in this study were done using solder checker equipment. Solder bump characterizations include bump height and uniformity, composition, shear force magnitude using solder bond analyser and bump profiles and cross section analysis were conducted using scanning electron microscopy.

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## REFERENCES

[1]. D. Manesis, and et al, (2004); Stencil Printing Technology for 100μm Flip Chip Bumping, *Global SMT and Packaging*, **4**, 10-14.
[2]. D. Manesis, and et al, (2006); Latest Technological advancements in Stencil Printing Processes for Ultra-fine-pitch Flip Chip Bumping Down to 60μm Pitch, *Proceedings on IMAP International.*
[3]. Stencil Printed Wafer Bumping – Cleaning, Kyzen Corporation, Manchester, (2001); in *http://www.flipchips.com/apnotes/kyzen/Kyzenstencilprinting.pdf*, (15/06/2007)
[4]. Y. Zhang, and et al, Lead-Free Bumping and Its Challenges, Transaction on IWLPC Proceedings in *http://www.enthone.com/docs/IWLPC804Zavarine.pdf*, (26/10/2007)
[5]. J. Kloeser, and et al, (2000); Low Cost Bumping by Stencil Printing: Process Qualification for 200μm Pitch, *Transactions on Microelectronics Reliability*, **40**, 497 – 505.
[6]. J.H. Adriance, (1999); Bumping of Silicon Wafers by Stencil Printing, *IEEE, International Electronics Manufacturing Technology Symposium*, 313-319.
[7]. Surface Mount Technology (SMT) – Step 4: Printing, in *http://smt.pennet.com/Articles/Articles_Display.cfm?Section*, (23/07/2007)

[8]. B. Huang, and C.N. Lee, Solder Bumping Via Paste Reflow For Area Array Packages, (2002); *IEEE Transactions on Electronics Manufacturing Technology Symposium, IEMT*, 1-17,

[9]. G.J. Jackson, R. Durairaj, and N.N. Ekere, (2002); Characterisation of Lead-Free Pastes for Low Cost Flip-Chip Bumping, *IEEE Transactions on Electronics Manufacturing Technology Symposium 2002*, 223-228.

[10]. L. Li, and P. Thompson, (2000); Stencil Printing Process Development for Flip Chip Interconnect, IEEE Transactions on Electronics Packaging Manufacturing, 23, 165-170.

[11]. R. W. Kay, and et al., (2005); Stencil Printing Technology for Wafer Level Bumping at Sub-100 Micron Pitch Using Pb-Free Alloys, IEEE, Electronics Components and Technology Conference, 848-854.

[12]. H.Z. Saadiah, and et al., (2007); Formulating Solder Fluxes and Solder Pastes or Flip Chip, Proceedings of the 1st NASPAC, 10-16.