Solid State Science and Technology, Vol. 16, No 2 (2008) 33-41
ISSN 0128-7389 Corresponding Author: wid_shualdi@yahoo.com 33

FAILURE ANALYSIS OF POWER MOS DEVICE FROM THE BACKSIDE OF THE DIE

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ABSTRACT

Backside analysis has been developed as a useful tool for failure determination for quite some time. This method of analysis, used for debug and fault isolation required a limitless stretch of the imagination and creative solutions. The procedures used to gain access to the back of the target die for backside Photoemission Microscopy have created many unique and challenging solution of their own. With the speed of change, advancement and developments within the power semiconductor technology, multi layer metallization and shrink processes make traditional front or top side analysis technique more difficult and in most cases impossible. Technological advancement results in utilization of backside analysis technique to become an important tool for debug and fault isolation.

http://journal.masshp.net/wp-content/uploads/Journal/2008/Jilid%202/W.M.S.W.%20Suliman%2033-41.pdf

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