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ELECTRICAL PROPERTIES OF POROUS SILICON PREPARED BY PHOTOCHEMICAL ETCHING

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ABSTRACT

In this work, electrical properties of porous silicon (PS) structure fabricated by using the photochemical etching process in HF acid under different etching times was investigated. (111) n-type silicon wafers with two different resistivities ($\rho_1 = 3.25 \times 10^{-4}$ Ωcm and ρ_2 = 4.3-5.6 Ωcm) were used. The wafers were etched in 40% HF acid by using 100 W quartz tungsten halogen lamp integral with ditchroic ellipsoidal mirror for two different etching times (t_1 = 1800 s and t_2 = 5400 s). The current-voltage characteristics for all Al/PS/n-Si/Al structures show a rectifying behavior with different values of ideality factor and barrier height. The forward and reverse current show Schottky-like behavior and the presence of an inflection point in reverse a characteristic is explained by energy band gap difference between porous silicon and crystalline silicon substrates.

INTRODUCTION

Porous silicon (PS) has been identified as a potential optoelectronic material, compatible with silicon technology after the discovery of strong room temperature photoluminescense (PL) from high porosity in 1990 [1]. Electriluminescense (EL) is also observed from a PS layer prepared by photochemical etching (Laser induced etching) and electrochemical etching under forward and reverse biasing [2-4]. PS consists of a network of nanometer-sized silicon regions surrounded by void space.
Many groups of researchers studied the electrical properties of PS prepared by electrochemical etching. According to Dimitrov [5], the I-V characteristics of porous silicon prepared by electrochemical etching is due to the existence of Schottky Junction between metal and PS interface while Pulsford et al. [7] and Ray et al. [8] believed that the I-V characteristics are due to heterojunction between PS and its silicon substrate. M. Ben-Chorin [6] et al. discussed the band alignment of p-type PS heterojunction in the light of PS/bulk silicon interface behaving like a Schottky diode, where the PS itself plays the role of metal. The photochemical etching (laser induced-etching (L.I.E.) technique is electrodeless without external potential, photon source as high power density laser is used to supply the required holes in the irradiated area of silicon wafer to initiate the etching [9]. Spectroscopic investigations of PS prepared by L.I.E were established to determine the silicon nanocrystallites sizes, size distribution and PL spectral [10, 11]. In this study, the electrical properties of porous silicon prepared using this technique have been investigated for Al/PS/n-Si/Al structure. The structures are

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based for different voltages and the resulting I-V characteristics have Schottky Junction-like behavior with different values of ideality factor and barrier height.

EXPERIMENTAL PROCEDURE

Photochemical etching technique is used in this study to prepare PS layer. Detailed information of this technique can be found elsewhere [12]. A commercially available n-type (111) oriented silicon wafer of two different resistivities ($\rho_1 = 3.25 \times 10^{-4}$ Ωcm and ρ_2 = 4.3-5.6 Ωcm) was rinsed with acetone and ethanol to remove grease and dirt and then immersed in electronic grade 40% HF acid. The mount of the wafer is in such a way that is explained in Ref. [12]. In this electrode less photochemical etching process, there was no applied bias. The light beam of quartz tungsten halogen lamp integral with dichroic ellipsoidal mirror, has been focused on a silicon wafer to a circular spot (1.13cm^2 area), the distance between the halogen lamp and the wafer about (4cm). Bubbles were observed during the etching process. Wafer were etching with different etching times, after which they were rinsed with ethanol and dried with nitrogen gas. The porous layer was formed on the side of wafer illuminated by halogen lamp.
Al electrodes are thermally deposited on the (3 x 3 mm^2) area of the irradiated surface of the wafers and on all back surface of the wafer. Electrical measurements are established in dark condition. The side view of the final device is shown in Figure.(1). For current-voltage measurements, two Keithley (616) digital electrometer and (50V) power supply are used. C-V measurements are achieved using a Fluke PM 6306 programmable automatic RCL meter. During capacitance measurements, the reverse voltage is varied from 0 to 5 V and the frequency is maintained at 1 MHz.

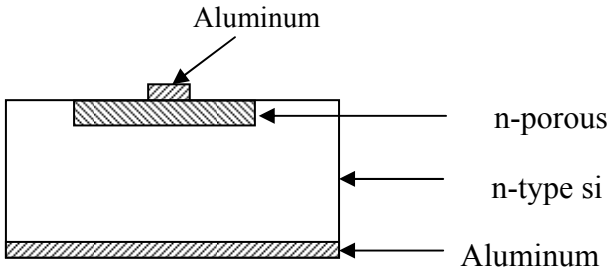

Figure 1: Sectional-view of the final device.

RESULTS AND DISCUSSION

I-V characteristics in dark conditions are done at room temperature on a number of Al/PS/n-Si/Al structures. Figure.(2) shows the I-V characteristics at two different etching times (t_1 = 1800 s and 5400 s) for silicon substrate resistivity of ρ_1.
The characteristics show a rectifying behavior with different rectifying ratios. The forward part of the measured I-V characteristics is similar to a Schottky diode characteristics, and may be analyzed using thermionic emission model [13]. From the slope of the semi-log I-V curve (not shown here), the ideality factor is larger than unity. The values of ideality factor are interpreted in [5] where its relation with the interface

states and to the possible thin insulator layer presented at the metal–semiconductor interface is given in the form:

$$n = 1 + \frac{\delta \in_s}{w \in_i} + \frac{\delta q D_S}{\in_i} \qquad (1)$$

where Ds is the density of localized states at the metal/PS boundary, w is the width of semiconductor space charge region and ε_S and ε_i are the dielectric constants of the interface and semiconductor region respectively. The I-V characteristics of Al/PS/n-Si/Al have been analyzed by a way similar to that described in [15]. We calculate the density of metal/porous silicon interface states by taking the values of $\varepsilon_S = \varepsilon_i$ and $\delta = 25^o$ as in [14, 15]. The obtained values for the ideality factor and barrier height are close to those given in [5, 16] for porous silicon prepared by electrochemical etching. The dependence of the I-V characteristics on the etching time is related to the formation of pores of porous silicon, where the pore diameter in porous silicon structure may be increased by increasing the etching time where the etching power is constant, which is led to increase the resistivity of porous silicon due to the carrier trapping at pores wall [6]; also the increasing of the etching time from t = 1800 s to t = 5400 s will lead to increase the thicknesses of the PS layer, where, a simple investigation under optical microscopy, allowed us to estimate the thickness of light-etched PS layer. We estimate a maximum depth of about 44 μm for etching time 1800 s and 78 μm for etching time 5400 s. the increasing in PS layer thickness will lead to increase the resistivity of PS layer [17].

Figure.(3) shows the current-voltage characteristics at two used resistivities (ρ_1 and ρ_2) and etching time of 1800 s. The dependence of (I-V) characteristics on the wafer resistivity is related to the effective charge carrier in PS layer after the etching process at a constant etching time and etching power. Results from I-V characteristics are summarized in Table (1). The reverse saturation current (I_S) is also tabulated in this table.

When we apply a forward bias to metal-semiconductor junction (metal side is positive and semiconductor side is negative), electron energy levels on the semiconductor side will increase by $q(V_{bi}-V)$, where V_{bi} denotes to the built-in voltage and V denotes to the applied forward bias voltage between metal and semiconductor. Therefore the Fermi energy level of semiconductor should be increased by the value of eV as well. Thus, barrier height for electrons passing from semiconductor to metal will be decreased by eV. As a result, current flow from semiconductor to metal will be increased by exp(eV/kT) at a constant etching time.

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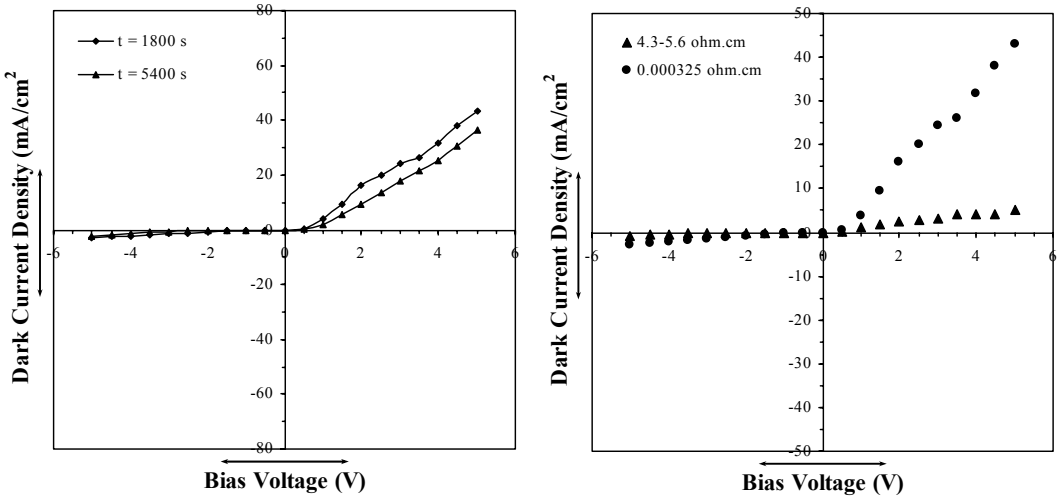

Figure (2): I-V characteristics of Al/PS/n-Si/Al structure at 1800 s etching time for two used resistivities.

The reverse current-voltage characteristics Table (1) of Al/PS/n-Si/Al structures are sensitive to the preparation condition for the wafers.
The dark current is related to the recombination-generation process associated with space charge region of Schottky Junction formed between the metal electrode and the porous silicon layer [5]. This current is observed even in the case of almost (PtSi-Si) Schottky diodes [18, 19]. The values of the current due to recombination-generation process depends only on the width of the depleted space-charge region (w) and described by:

$$J = B\sqrt{V - V_{bi}} \qquad (2)$$

where $B = q\frac{n_i}{\tau_o}\left[\frac{2 \in_s \in_o}{qN_D}\right]^{1/2}$ (2)

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Table (1): Values obtained from I-V measurements.

Etching time (s)	Resistivity Ωcm	I_S (μA/cm^2)	**n**	Φ_{bn} (eV)	Ds(cm^{-2}ev^{-1})
1800	3.25 x 10^{-4}	58	9.6	669	2.26 x 10^{14}
5400	3.25 x 10^{-4}	27	10.2	686	2.42 x 10^{14}
1800	4.3-5.6	100	13.5	653	3.28 x 10^{14}

Reciprocal of C^2 against V is plotted in Figure.(4). The plot is illustrated as a straight line which indicates an abrupt type. The effective carrier density (N_D) and depletion layer width (W) that is calculated from this curve is listed in Table (2).

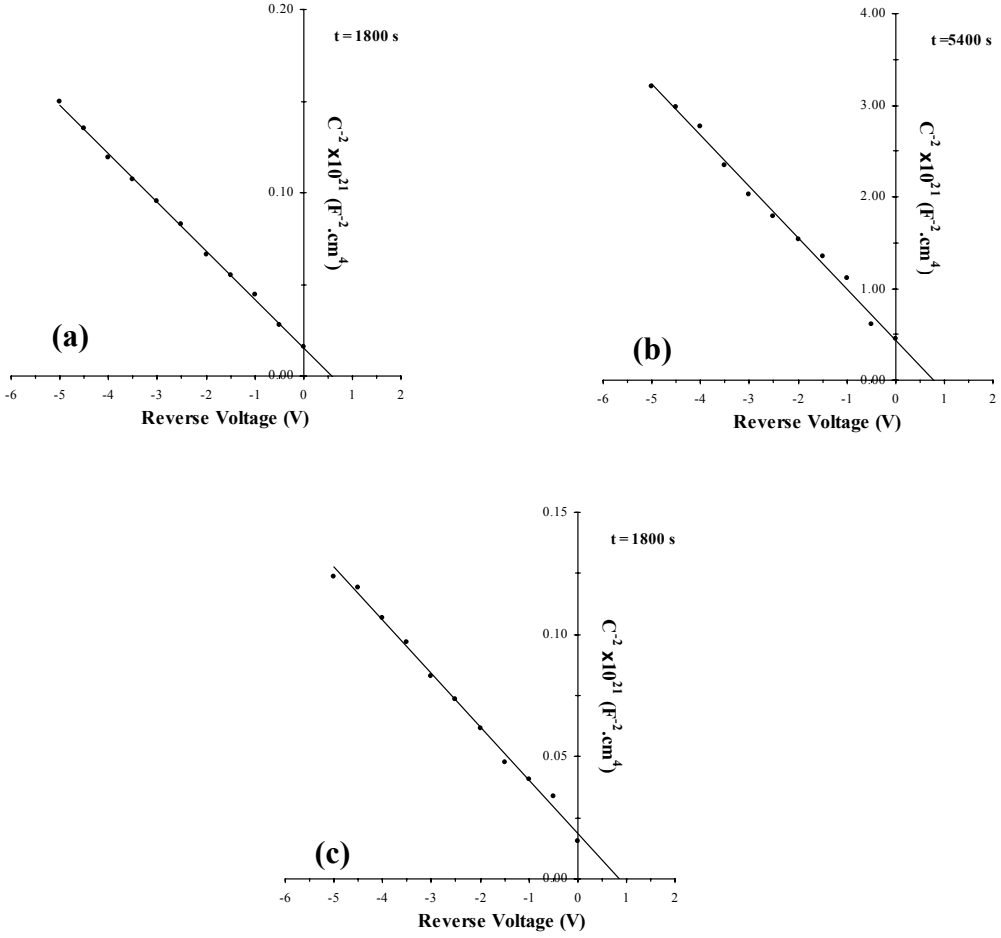

Figure 3: C^{-2}-V plot; (a) and (b) for ρ_1 and (c) for ρ_2.

Table :2 Values obtained from C-V measurements

Etching time (s)	Resistivity Ωcm	N(cm^{-3})	$W(\mu m)$
1800	3.25×10^{-4}	4.7×10^{13}	5.3
5400	3.25×10^{-4}	2.6×10^{13}	5.9
1800	4.3-5.6	1.7×10^{12}	23

CONCLUSIONS

The Al/PS/n-Si/Al structure in this work is a Schottky-like junction with high ideality factor due to the formation of high density of interface states at PS boundaries. The junction is an abrupt type.

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