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JUNCTION LEAKAGE OF A SiC-BASED NON-VOLATILE RANDOM ACCESS MEMORY (NVRAM)

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ABSTRACT

The potential for developing a one-transistor one-capacitor (1T–1C) nonvolatile random-access memory (NVRAM) on 4H SiC is experimentally investigated in this paper. Using a metal–dielectric–metal (MOM) capacitor as the memory element and a MOSFET on SiC as the select transistor, the charge loss due to the carrier generation, contributing to reverse-biased *pn* junction leakage, can be slowed down to the levels that convert this memory cell into practically nonvolatile. Test metal–oxide–semiconductor (MOS) structures on 4H SiC are used to experimentally determine the time that is needed for the surface generation to create the MOS inversion layer at high temperatures. This relaxation time can then be used to *estimate* the retention time in the NVRAM cell. The calculated charge-retention times for NVRAMs fabricated on n- and p-type substrates are in the orders of 10^{19} s and 10^{18} s, respectively.

INTRODUCTION

Semiconductor memory is a generic logic device which enables binary digit (bit) data to be stored and manipulated. It can be broadly divided into two types, i.e. volatile and non-volatile memory. Data of the former type of memory would not be retained when power supplied is removed. In contrast, nonvolatile memory is having the ability to retain data for a period longer than 10 years, at temperatures as high as 80^{o}C, even power supply is disconnected. The global demand of this type of memory is increasing, mainly due to the growing number of portable, compact, and light-weigh electronic appliances [1].

Conventional silicon-based nonvolatile-semiconductor memories only associated with read-only-memory (ROM) elements, for example flash memory. These devices can only withstand limited (about 10^{6}–10^{7}) charging/discharging cycles, with too long charging/discharging times, to allow their use for random-access memory (RAM) applications [1]. RAMs, such as dynamic RAM (DRAM), use metal-oxide-semiconductor (MOS) capacitor as storage element. They respond very quickly (nanoseconds) during charging/discharging cycles, but they are volatile and need refreshing (every tens of millisecond) in order to maintain the stored data. This is a disadvantage for portable, light-weight, and low power consumption gadgets. As a result, many researchers are motivated to find ways and means to develop a next generation nonvolatile memory (giant magnetoresistance RAM, ferroelectric RAM,

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ovonic unified memory, etc.) [2]. Silicon carbide (SiC) is an emerging material that has superb intrinsic properties, such as extremely low thermal generation rate (according to the first order of Shockley-Read-Hall model) [3] and the ability to fabricate an acceptable quality of SiC-based MOS capacitors [4], theoretically enabling *nonvolatile random-access memorie*s (NVRAMs) — memory elements with access characteristics of silicon RAMs and with retention characteristics of silicon read-only memories (ROMs) — to be made. The proposed SiC-based NVRAM is a combination of a select transistor and a capacitor (1T–1C), similar to the 1T–1C Si-based DRAM structure [5]. The possible leakage mechanisms, which contribute to the volatile characteristics of the memory, in these structures are assumed to be the same, except that the substrates are different. Figure 1 [6] shows the potential leakage mechanisms of a select p-channel metal-oxide-semiconductor field-effect (MOSFET) integrated with a SiC-based MOS capacitor: (1) leakage through the dielectric of the storage MOS capacitor, (2) electron-hole generation in the depleted region of the storage MOS capacitor, (3) junction leakage due to electron-hole generation in the depletion layer surrounding the drain region of the select MOSFET, (4) leakage through the select MOSFET due to its subthreshold current, (5) tunneling current through the gate dielectric of the select MOSFET, and (6) band-to-band tunneling at the edge of the select MOSFET [or gate-induced drain leakage (GIDL)].

The potential of developing a 1T–1C NVRAM on 4H, and 6H SiC has been experimentally investigated [6]-[10]. From literatures, the investigations were only concentrated on two possible leakage paths [(1) to (2)]. MOS capacitors fabricated on SiC with nitrided oxide–semiconductor interfaces [9] were used in these investigations, either as memory elements themselves or as test structures. Table 1 [6]-[10] summarizes the charge-retention times of the two possible leakage paths. There was no report on the remaining leakage paths. Therefore, in this paper, effect of thermal-generation current in a reverse-biased *pn* junction surrounding the drain region of a select MOSFET, which is associated with the third leakage mechanism, will be investigated using mathematical analysis method based on the available experimental data.

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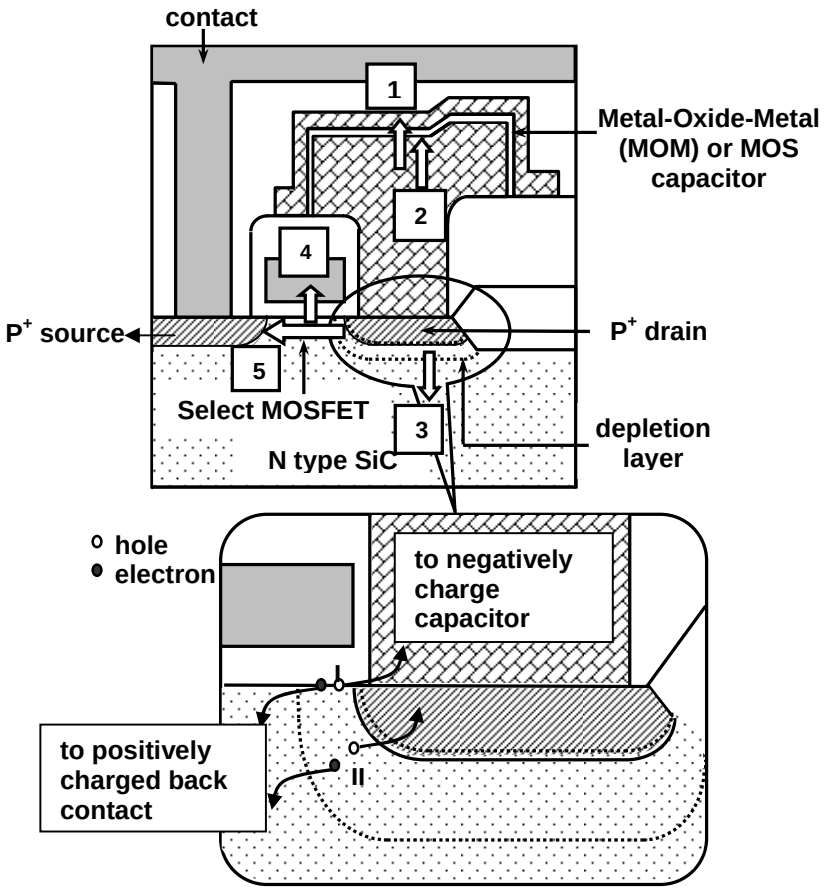

Figure 1: Various possible leakage mechanisms in a proposed SiC-based 1T–1C NVRAM cell. The numbered leakage paths have been explained in the text.

Table 1: Estimated room-temperature charge-retention times deduced from different leakage paths.

Leakage Path	Charge-retention time (s)	
	N-type 4H SiC	P-type 4H SiC [a]
1[b]	8×10^{12}	3×10^{12}
2	1×10^{17}	1×10^{16}

[a] a positive voltage is applied to the surrounding of the capacitors (MOS capacitor with a shielding ring) [5]-[9]. [b]: measured by floating-gate technique [5], [10].

SAMPLE PREPARATION

To conduct this investigation, 4H SiC-based MOS capacitors acting as test structures are used. Si-faced, n- and p-type 4H–SiC wafers were used to fabricate MOS capacitors on 3-μm thick epilayers oriented 8^{o} off (0001) direction that were purchased from CREE Research Inc. Nitrogen and aluminum were used as n- and p-type dopants, the

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concentrations of both dopants were being (0.70-1.10)×10^{16} cm^{-3}. The wafers were first cleaned in a mixture of H_2SO_4 and H_2O_2, followed by an RCA clean. Immediately prior to oxide growth, the wafers were dipped in 1% HF for 1 min. Then, they were inserted into a horizontal quartz furnace to grow nitrided gate oxides by *sandwich* technique [9]: initially the oxides were directly grown in 100% nitric oxide (NO) for 1 hour at 1175^{o}C, followed by 2 hours 30 min of dry oxidation, and final 2 hours of direct 100% NO grown. After the oxide growth, the samples were cooled down to 800^{o}C in high-purity N_2 at approximately 5^{o}C/min. The subsequent processing steps have been described elsewhere [14].

CHARGE-RETENTION MEASUREMENTS AND DISCUSSION

The SiC-based 1C–1T NVRAM cell consists of a memory capacitor and a select MOSFET that supplies and controls the stored charge in the capacitor (Fig. 1). The capacitor can be either metal–dielectric–metal or metal–oxide–semiconductor (MOS). When the capacitor is charged, the drain–body *pn* junction is reverse-biased, with a depletion layer surrounding the junction [11]. Electron-hole pairs are generated in the depletion layer, either in the bulk and/or at the semiconductor–oxide interface (labeled as I and II in Fig. 1). The generated electron-hole pairs are then separated, as they are attracted to the opposite-polarity charge in the capacitor and in the bulk contact. Therefore, a generation current is established that discharges the capacitor. This type of charge loss is identified as one of the leakage mechanisms that cause the volatile nature of Si-based DRAMs. In fact, if a metal–oxide–metal (MOM) capacitor with negligible leakage through the dielectric were used, the generation current would be the dominant leakage mechanism. According to the first order of Shockley-Read-Hall model [3], the generation rate is related to the intrinsic-carrier concentration (n_i). Given that n_i in 4H SiC is about 1.6×10^{-7} cm^{-3}, which is approximately 17 orders of magnitude lower than in Si, the generation rate in 4H SiC should be many orders of magnitude lower than in Si. Therefore, the above-mentioned discharge mechanism could be practically eliminated using 4H SiC as the material for the select MOSFET. The time needed to discharge a non-leaky MOM capacitor via the generation current of the select transistor can be related to the relaxation time, τ, of a test MOS capacitor. Assuming similar doping levels and biasing, linear scaling of the areas and the capacitor charge leads to the following relationship between the charge-retention and the capacitor-relaxation times [5]:

$$t_{ret} = \left(\frac{\Delta Q_{DRAM} A_{test}}{\Delta C_{test} |V_r| A_{MOSFET}} \right) \tau \qquad (1)$$

where, t_{ret} is the charge-retention time of a SiC-based 1C–1T NVRAM cell (as determined by the generation current in the select MOSFET), ΔQ_{DRAM} is the stored charge in the capacitor of the cell (typically, 20 fC in a Si-based 1T–1C DRAM [12]), $|V_r|$ is the drain–to–body reverse bias created by the charged memory capacitor, A_{MOSFET} is the surface area of the drain–to–bulk depletion layer, A_{test} is the area of the test structure (MOS capacitor), ΔC_{test} is the difference in capacitance between C_{dd} and C_{inv} (Fig. 2) [8] and τ is the relaxation time of the test-MOS capacitor.

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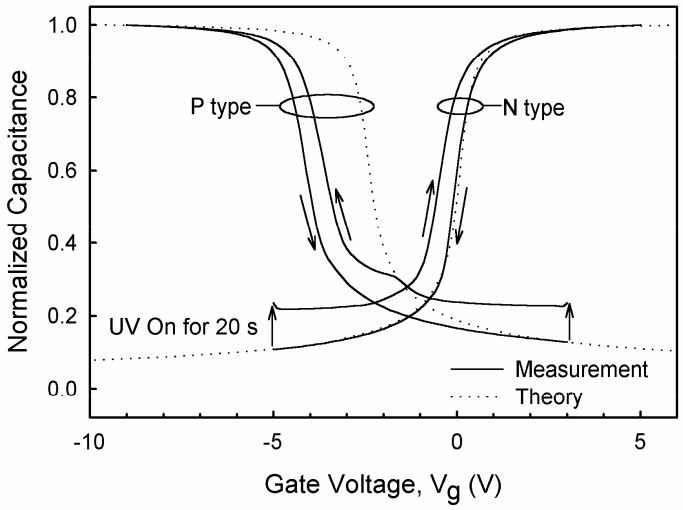

Figure 2: Typical high-frequency capacitance-voltage measurements at dark conditions and illuminated after UV light of MOS capacitors on n- and p-type 4H SiC. Arrows indicate sweeping direction [8].

The estimated relaxation time, τ, of the measured n- and p-type (with shielding ring) MOS capacitors, with area A_{test}=1.35×10^5 μm^2, were 10^{17} s and 10^{16} s, respectively. These are similar to the second leakage path shown in Fig. 1 and reported in ref. [5]-[9]. Assuming that the carrier concentrations in the p$^+$ drain and n substrate are 10^{18} cm^{-3} and 10^{16} cm^{-3}, respectively; the calculated built-in voltage for the *pn* junction is 2.5 V, and the resulting depletion width of n- and p-type substrates are 0.31 μm and 0.32 μm at a reverse-biased voltage, $|V_r|$,=5.2 V and 5.5 V, respectively. The lateral depletion width is assumed to be identical to the vertical depletion width [13], so, for a 1-μm^2 p$^+$ drain, the A_{MOSFET} is approximately 1.67 μm^2 for both n and p-type substrates. Using the room temperature value of τ and ΔC_{test}=9.9 pF (for n-type SiC) and 7.2 pF (for p-type SiC), the calculated charge-retention time, t_{ret}, for n- and p-type substrates are in the orders of 10^{19} s and 10^{18} s, respectively. This demonstrates that the NVRAM cell will be practically nonvolatile when the select MOSFET is implemented into 4H SiC and a non-leaky metal–oxide–metal capacitor is used.

CONCLUSION

In this paper, the junction leakage due to electron-hole generation in the depletion layer surrounding the drain region of a select MOSFET in a 1T–1C NVRAM cell with a non-leaky metal-oxide-metal capacitor has been investigated. The extracted memory retention times were in the orders of 10^{19} s and 10^{18} s, for the respective n- and p-type SiC substrates.

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