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SIMULATION OF NON-VOLATILE MOS MEMORY USING Si QUANTUM DOT WITH Ge CORE AS ELECTRONICS STORAGE NODE

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ABSTRACT

The MOS memory using Si quantum dot with Ge core as a floating gate has been discussed and improved. The major concern of using Ge core cladding by Si nanocrystals is to enhance the carrier confinement effect since the energy gap of Ge is narrower than that of Si, a compound well could be formed in the center of the dot and the charge could be stored mainly in the side of Ge core. As the result, the retention time could be increase significantly without deteriorating the writing/erasing speed. The simulation shows that the flash memory with the dot size of 9-12nm in diameter possesses a retention time up to 10^9 or about ten years with a 2nm-thick tunnel oxide, while the writing and erasing time is at the order of μs which is similar to that of the memory based on pure Si quantum dot. Moreover, cladding Ge by Si nanocrystal allows us to keep the good Si-SiO_2 interface instead of poor Ge-Oxide interface.

INTRODUCTION

Metal-oxide-semiconductor field-effect transistor (MOSFET) memories based on nanocrystals have been considered as a most promising application of nano-scale devices in future VLSI. Some group research [1-6] have discussed the advantages of high density, low power, multiple threshold and the comparability to logic circuit. In this kind of memory, nanocrystals embedded in SiO_2 layer and the charges inject into nanocrystals via direct tunneling and as a result the threshold of the devices changes. In general, the thickness of direct tunneling oxide is one of the important factors. Decreasing the thickness can improve writing/erasing time, but this result in the degradation of the charge storage. In contrast, increasing the thickness is useful for retention time but not for writing/erasing time. In order to overcome this problem, a novel MOSFET memory storage node was proposed using Si dots with Ge core instead of the pure Si nanocrystals [7]. The major concern of Ge core cladding by Si nanocrystals is to enhance the carrier confinement effect since the energy gap of Ge (0.66 eV) is narrower than that of Si (1.12 eV), a compound could well be formed and the charge could be stored mainly in the side of Ge core. As the result, the retention time could be increased significantly, at the same time; the writing/erasing time would be the same value with Si quantum dot case. Hence, this kind of memory is expected to have the advantages both of high-speed programming and long retention time. Moreover, Ge core cladding by Si allows us to keep the good Si/SiO_2 interface instead of poor Ge/SiO_2 interface.

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In the previous work, we have demonstrated the formation of Si dots with Ge core on the ultrathin SiO_2 by alternately controlling the selective growth conditions in LPCVD using pure SiH_4 and GeH_4, and we found the highly selective growth of Ge on the pregrown Si dots and subsequent complete coverage of Si cap [8]. Also, the structural and electrical properties of Si quantum dot with Ge core have been studied systematically [9-11].

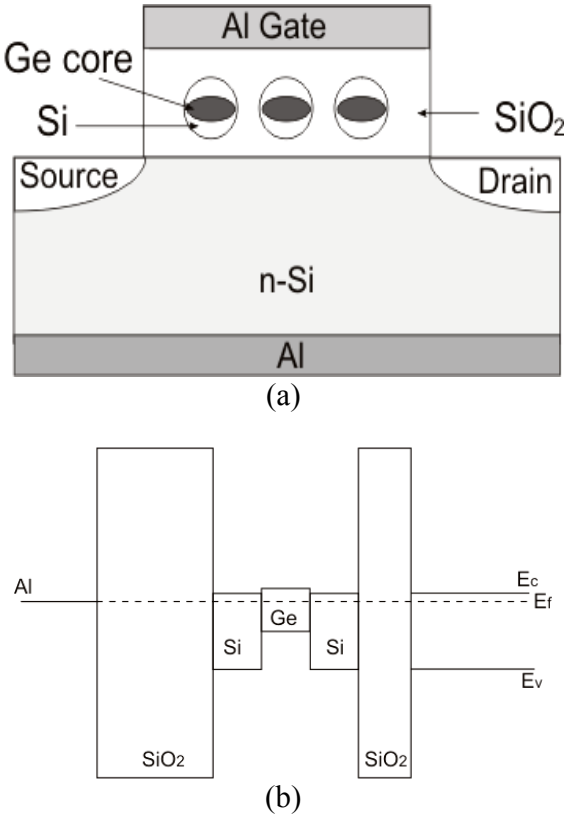

Figure 1: Schematic diagram of the memory device using Si dot with Ge core as floating gates (a) accompanied with their energy band structure (b).

In this work, we present our physical model, which is extended to include the quantum confinement effect on the energy level of the hetero-nanocrystal, the thermal activation of the trapped hole in the nanocrystal, as well as the electron current during erasing. Numerical simulation concerning retention and operation time will be carried out to gain the better understanding of the important role of the Ge core. This model is believed to predict more reliable device operation results of a real device.

EXPERIMENTAL

The schematic diagram of MOS memory using Si quantum dot with Ge core as floating gate is shown in Figure 1 (a). The dot shape is spherical consisting of the Si clad and

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ellipsoidal Ge core, this is caused by the local strain emerged by the lattice constant misfit between Ge and Si [7]. We vary the diameter of Si clad and Ge core as well as oxide thickness (SiO_2) to investigate tunneling process for memory operation speed and its retention time. Figure 1(b) shows the energy band diagrams of cross sectional Si/Ge/Si dot memory cell. The carrier transport in memory operation of such quantum dot memory occurs when the bias voltage is applied between the control gate and the substrate.

There are two main parameters which will be calculated in this study i.e: (1) programming speed (includes writing and erasing time) and (2) retention time. We will start with the time concept in memory device, which can be defined as the inverse of the tunneling current density [12-13], that is

$$t = \frac{q}{J.L^2} \tag{1}$$

where q, J, and L are the electron charge, tunneling current densities, and the linear size of nanocrystal, respectively.

The writing and erasing tunneling current densities are calculated using the method proposed in [14, 15], considering the quantization of carriers in the inversion layer or the accumulated layer when the device is biased

$$J = q \int_{E_{\text{shift}} \le E} D(E) f(E) \rho(E) F(E) dE \tag{2}$$

$f(E)$ is the impact frequency, $\rho(E)$ is the 2-D density of states, $F(E)$ is the Fermi-Dirac distribution function, and $D(E)$ is the tunneling probability. E_{shift} is the Si valence (for writing) or conduction band (for erasing) shift due to quantum confinement effect from the small size of the nanocrystal. The impact frequency reads [15]

$$f(E) = \frac{1.2q}{(3\pi\,\eta\, m_{\text{Si},\perp})^{1/3}} \left(\frac{\varepsilon_{\text{ox}} V_{\text{ox}}}{\varepsilon_{\text{Si}}} \right) \tag{3}$$

Where η, $m_{\text{Si},\perp}$, ε_{ox}, V_{ox} and ε_{Si} are the reduced Planck's constant, the hole (or electron) effective mass perpendicular to the substrate, the dielectric constant of SiO_2 layer, the surface electric field in the SiO_2 layer, and the Si dielectric constant, respectively. The density of states for a 2-D confined hole or electron gas is

$$\rho(E) = \frac{m_{\text{Si},\perp}}{\pi\,\eta^2} \tag{4}$$

The tunneling probability $D(E)$ can be calculated using transfer matrix method [16]. The potential barrier is split up into some segments, which potential energy can be regarded as a constant. In the limit as the divisions become finer and finer, a continuous variation will be recovered. Using the boundary conditions and continuity, we can determine the amplitudes of the forward and backward wave components in the *i*-th

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slice, A_i and B_i. By setting $A_0 = 1$ and $B_{N+1} = 0$, for $i = N + 1$ we can calculate the transmission amplitude A_{N+1} and the tunneling probability as follows:

$$A_{N+1} = \frac{m^*_{N+1}}{m^*_0}\frac{k_0}{k_{N+1}}\frac{1}{M_{22}} \tag{5}$$

and

$$D(E) = \frac{m^*_0}{m^*_{N+1}}\frac{k_{N+1}}{k_0}\left|A_{N+1}\right|^2 \tag{6}$$

where M_{22} is the 22-element of final matrix obtained from the calculation method derived in [11] and k_i is the wave vector in the i-th slice.

Memory retention time t then can be obtained with following method:

$$t = \frac{1}{\sum_{i=1}^{\infty}\exp\left[-\frac{(E_i - E_0)}{k_B T}\right]f(E_i)D(E_i)} \tag{7}$$

E_i, E_0, and k_B are respectively the i-th excited ground states of hetero-nanocrystal and Boltzmann's constant. The integer number n is the quantum number from which the wave function of the hole covers both Ge and Si regions of the hetero-nanocrystal. And for all calculations, the control oxide is fixed at 3 nm-thick so the tunneling through control oxide can be neglected.

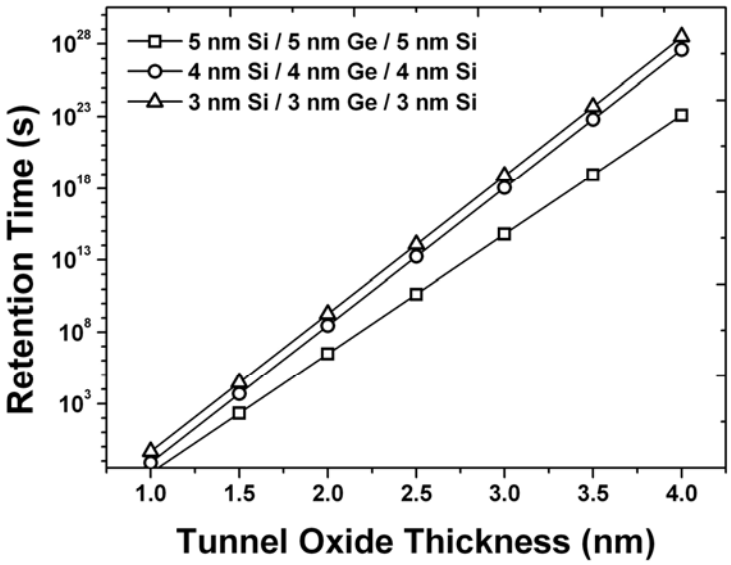

Figure 2: Retention time of Si/Ge/Si dot memory as function of tunnel oxide thickness.

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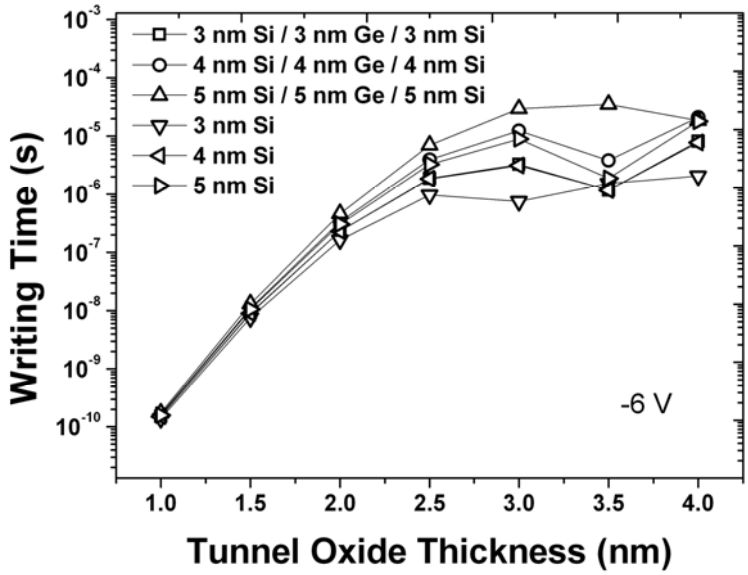

Figure 3: Writing time of both Si/Ge/Si dot and Si nanocrystal memory as function of tunnel oxide thickness.

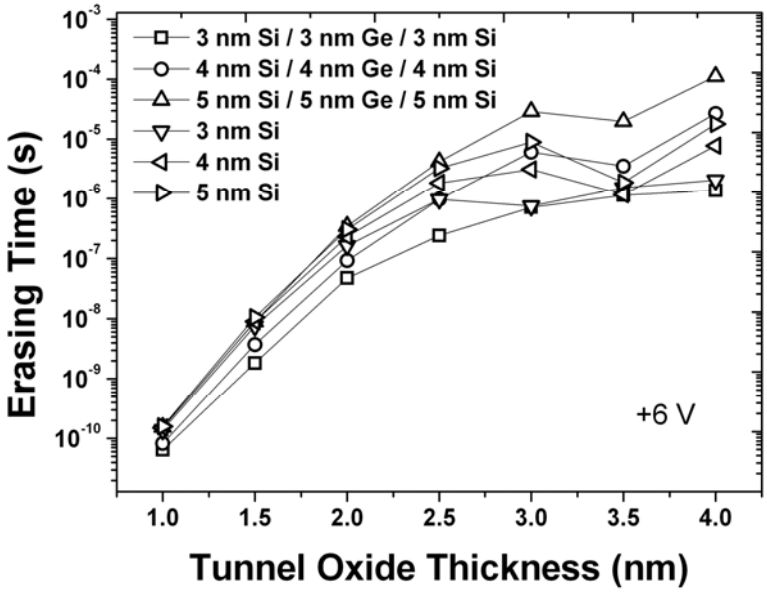

Figure 4: Erasing time of Si/Ge/Si dot and Si nanocrystal memory as function of tunnel oxide thickness.

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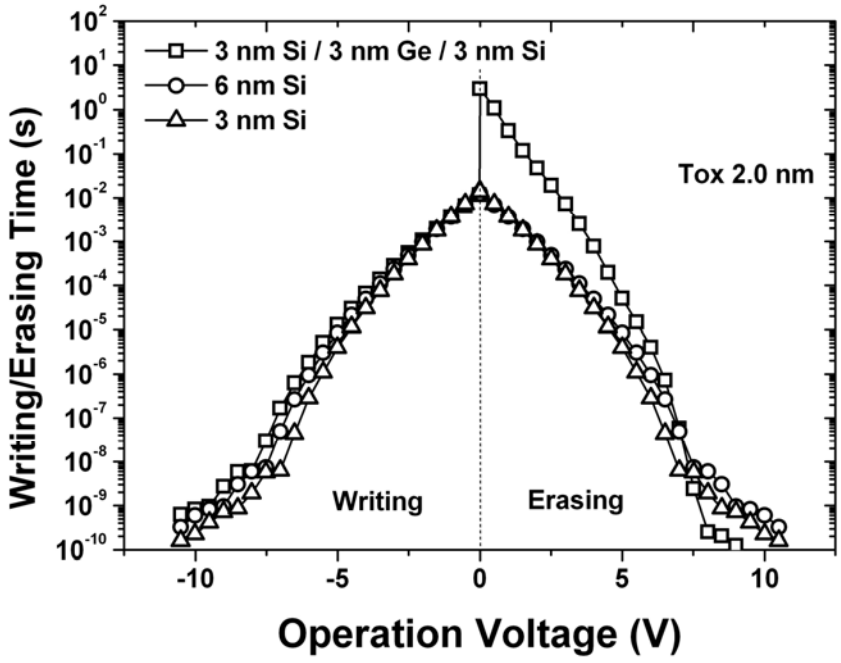

Figure 5: Writing and erasing time of both Si/Ge/Si dot and Si nanocrystal memory as function of operation voltage.

RESULTS AND DISCUSSIONS

The retention time for both Si/Ge/Si dot memory as function of tunnel oxide thickness is shown in Figure 2. The retention time gets longer as the thickness of tunnel oxide increases. As a comparison, the retention time of Si/Ge/Si memory at 2 nm-thick tunnel oxide and 15 nm-height Si/Ge/Si dot reaches up to 10^9 s or around ten years. This shows that Ge core plays its important role in increasing the retention characteristic of the memory. In Si/Ge/Si memory, during the retention mode, hole is confined in Ge potential well and also there are Si and oxide barrier those block holes to tunnel back to the substrate.

The writing time as function of the tunnel oxide thickness for both Si/Ge/Si dot and pure Si dot memory operating at -6 V is given in figure 3. Writing time tends to increase as tunnel oxide thickness increases due to lower tunneling probability of carrier in thicker tunnel oxide. In range of tunnel oxide thickness lower than 2 nm, we found that the writing time of Si/Ge/Si dot memory reaches the value as well as that of pure Si dot memory while the results vary in range over 2 nm-thick tunnel oxide. Figure 4 shows the erasing time as function of the tunnel oxide with an operation voltage of +6 V. Erasing time increases as well as writing time if the tunnel oxide thickness increases. Both Si/Ge/Si dot and Si dot memory give erasing time around 10^{-6} s at 2.5 nm-thick tunnel oxide with small deviation. The results show that the influence of embedding Ge core to Si dot in both writing and erasing speed can be disregarded.

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The comparison between writing and erasing time as function of operation voltage are given in figure 5. The figure shows the dependence of memory operation time to operation voltage. Writing time of both Si/Ge/Si dot and pure Si dot memory increases while the erasing time decreases as operation voltage increases. However, there is almost no significant deviation between Si nanocrystal memory with and without Ge nanocrystal.

CONCLUSIONS

The important role of Ge-core in Si quantum dot memory regarding the improvement of devices performance has been simulated. The simulation results give significant value of retention characteristic up to 10^9 s while memory operation speed is less than μs. This quantum dot memory using Si quantum dot with Ge core has the potential advantage of fast write and erase time, low voltage operation, and long retention characteristic that make it as a promising candidate for novel memory device.

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