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SCALING AND NUMERICAL SIMULATION ANALYSIS OF 50nm MOSFET INCORPORATING DIELECTRIC POCKET (DP-MOSFET)

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ABSTRACT

Characterization of a metal-oxide-semiconductor field effect transistor (MOSFET) incorporating dielectric pocket (DP) for suppression of short-channel effect (SCE) was demonstrated by using numerical simulation. The DP was incorporated between the channel and source/drain of planar MOSFET and was scaled to get an optimized structure. An analysis of current-voltage (I-V) of 50 nm channel length (L_g) has been done successfully. The DP has suppressed short channel effect (SCE) without the needs of decreasing the junction depth. A reduction of leakage current (I_{OFF}) was obtained in MOSFET with DP without altering the drive current (I_{ON}). A very low leakage current is obtained for DP device with drain voltage (V_{DS}) of 0.1 V and increase when V_{DS} = 1.0 V. Consequently, the threshold voltage (V_T) is increased accordingly with the increasing of body doping. A better control of V_T roll-off was also demonstrated better for MOSFET with DP as compared to conventional MOSFET. Thus, the incorporation of DP will enhance the electrical performance and give a very good control of the SCE for scaling the MOSFET in nanometer regime for future development of nanoelectronics product.

INTRODUCTION

The Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) has been a popular device as it is extensively used in digital circuits, microprocessors, memory circuit, and other logic applications of many kinds. In order to improve the packing density and device performance in ultra-large scale integrated (ULSI) circuits, MOSFETs have been scaled down successfully over the past few decades. However, continued scaling faces challenges such as lithography and short channel effects [1]. Consequently, ultra-shallow source/drain junctions with high conductivity are necessary as the device is scaled down to 50 nm and below [2].

In current deep submicron MOSFET technology, pocket implantation appears to be a commonly used strategy for suppressing short-channel effects (SCE) [3]. However, there are many inconveniences such as an increase of the body factor and junction capacitance as well as the junction leakage current. Besides, high doping increases the risk of avalanche breakdown at the drain/substrate junction. Another problem relating to pockets consists of an increase of threshold voltage fluctuations that they induce. Instead of reducing the junction depth, dielectric pockets that limit dopant diffusion in planar MOSFETs have been proposed [4]. This achievement is able to overcome all of

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the above-mentioned problems and efficiently suppresses SCE.

In this paper, characterization of a metal-oxide-semiconductor field effect transistor incorporating dielectric pocket (DP) for suppression of short-channel effect (SCE) is demonstrated by using numerical simulation. An analysis for 50nm channel length (L_g) and different scaled of DP that incorporated between the channel and source/drain with selected uniform body doping of 10^{18} cm^{-3} has been done successfully [5]. The DP has suppressed short channel effects (SCE) such as a reduction of leakage current (I_{OFF}) without altering the drive current (I_{ON}), low leakage current is obtained for DP device with drain voltage (V_{DS}) of 0.1V and a better control of V_T roll-off was also demonstrated better for MOSFET with DP as compared to conventional MOSFET. Thus, the incorporation of DP will enhance the electrical performance and give a very good control of the SCE for scaling the MOSFET in nanometer regime for future development of nanoelectronics product.

EXPERIMENT DETAILS

The device structure is designed and simulated using SILVACO (ATLAS) software package. Figure 1 explicitly shows the simulated device structure with all the dimension of respective regions. The device consists of a silicon semiconductor substrate with uniform boron doping of 10^{18} cm^{-3} on which a thin layer of insulting oxide (SiO_2) of thickness t_{ox} = 2nm is grown. A conducting layer called the polysilicon gate electrode is deposited on top of the oxide. The gate is heavily doped with phosphorus of 10^{20} cm^{-3}. Two heavily phosphorus doped regions of 10^{20} cm^{-3} with depth X_j = 100nm, called the source and the drain are formed in the substrate on either side of the gate. The source and the drain regions overlap slightly with the gate. The channel length region of 50nm is designed for an analysis of the characteristics. The width and height of the dielectric pockets will be scaled in different sizes to get an optimize structure. A heavily dense mesh is needed in critical regions such as channel, DP area and gate oxide for accurate characterization of the device.

The inversion layer mobility model from Lombardi [6] was employed for its dependency on the transverse field (i.e field in the direction perpendicular $E_\perp$ to the Si/SiO_2 interface of the MOSFET) and through velocity saturation at high longitudinal field (i.e field in the direction from source-to drain parallel E to the Si/SiO_2 interface) combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models [6]. This recombination model was selected since it takes into account the phonon transitions effect due to the presence of a trap (or defect) within the forbidden gap of the semiconductor. An interface fixed oxide charge of $3x10^{10}$ Coulomb is assumed with the used of n-type Polysilicon gate contact for the device. The Drift-Diffusion transport [9] model with simplified Boltzmann carrier statistics [6] is employed for numerical computation of the design device.

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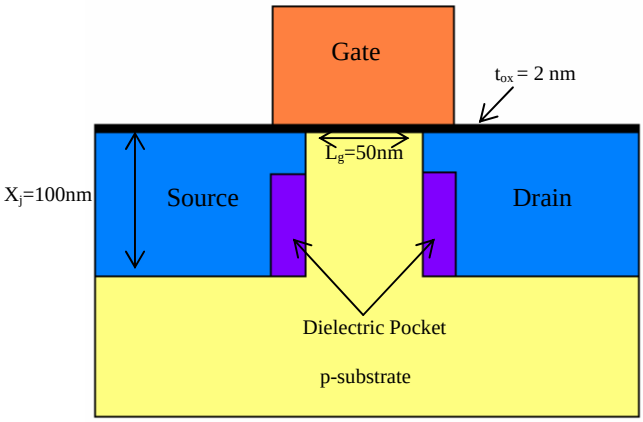

Figure 1: Schematic structure of NMOS device with dielectric pockets.

RESULTS AND DISCUSSION

The combination of Gummel and Newton numerical methods [6] was employed for a better initial guess in solving quantities for obtaining a convergence of the device structure.

Current-Voltage ($I_{DS} - V_{GS}$)
Figures 2 and 3 show the current-voltage ($I_{DS} - V_{GS}$) characteristics and subthreshold curves for DP-MOSFET device of channel length L_g = 50nm with different scale of DP and uniform boron doping of 10^{18} cm^{-3}. In Figure 2, the V_T is increased in magnitude from the structure of DP of 30x70, 40x70, 30x80, 40x80, 20x70 and to 20x80. With the DP existed between S/D regions, the SCE is controllable and the device was behaving more to NMOS rather than PMOS for channel length of 50nm respectively.

In the off-state operation mode the transistor shows a drain leakage current I_{OFF} which is independent of the gate voltage, but decreases from the structure of DP of 30x70, 40x70, 30x80, 40x80, 20x70 and to 20x80 as depicted in Figure 3. The highest, middle and lowest I_{OFF} are calculated from DP structure of 30x70, 30x80 and 20x80 respectively. With DP incorporation, a very low off-state leakage current (I_{OFF}) and good drive current (I_{ON}) taken at V_{DS} = 0.1V was explicitly shown. Due to the dielectric pockets, the off-state current can be significantly reduced. The reduction in the SCEs in the devices with dielectric pockets explains the difference in the threshold voltages of measured short-channel devices. Slight increase of drive current, I_{ON} is obtained in devices with DP. In other words, for scaling the channel length beyond the nanometer regime, the DP is essential for controlling the aggravated of SCE and setting properly the V_T [7].

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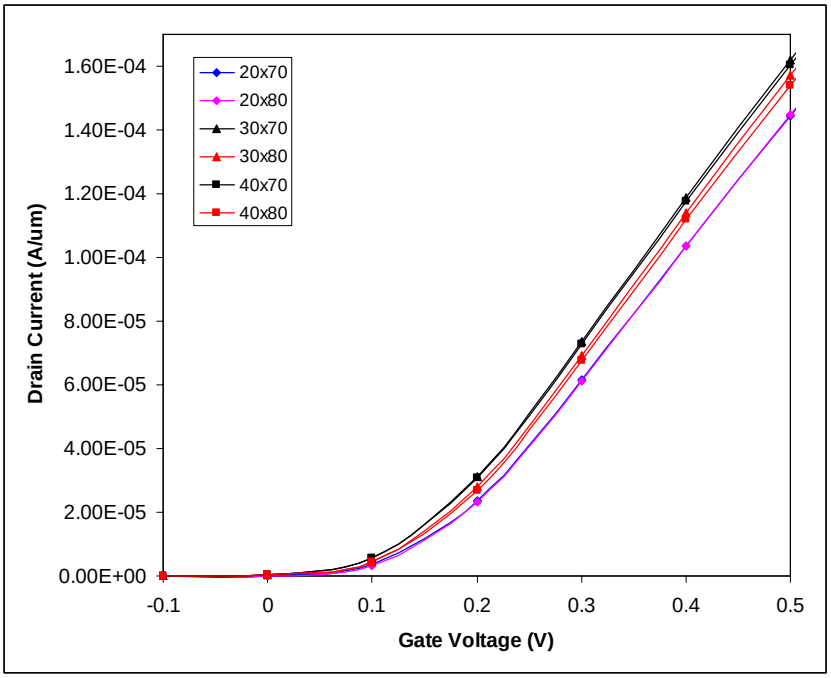

Figure 2: Current-Voltage (I_{DS} – V_{GS}) characteristics of 50nm DP-MOSFET with different scaled of DP and uniform boron doping of 10^{18} cm^{-3}.

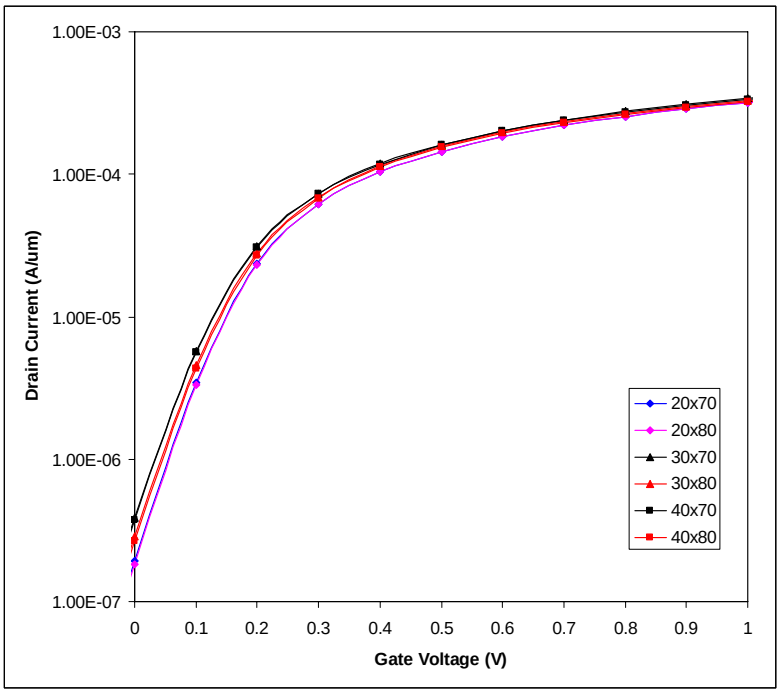

Figure 3: Subthreshold curves of 50nm DP-MOSFET with different scaled of DP and uniform boron doping of 10^{18} cm^{-3}.

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Output ($I_{DS} - V_{DS}$)
An output characteristic of the 50nm DP-MOSFET transistors with different scale of DP and uniform boron doping of 10^{18} cm^{-3} are shown in Figure 4. The gate voltage is 1.1V. These characteristics serve to demonstrate the enhanced performance that can be obtained using DP concepts. The drain current is decreased from the structure of DP of 30x70, 40x70, 30x80, 40x80, 20x70 and to 20x80. The highest, middle and lowest drive current are calculated from DP structure of 30x70, 30x80 and 20x80.

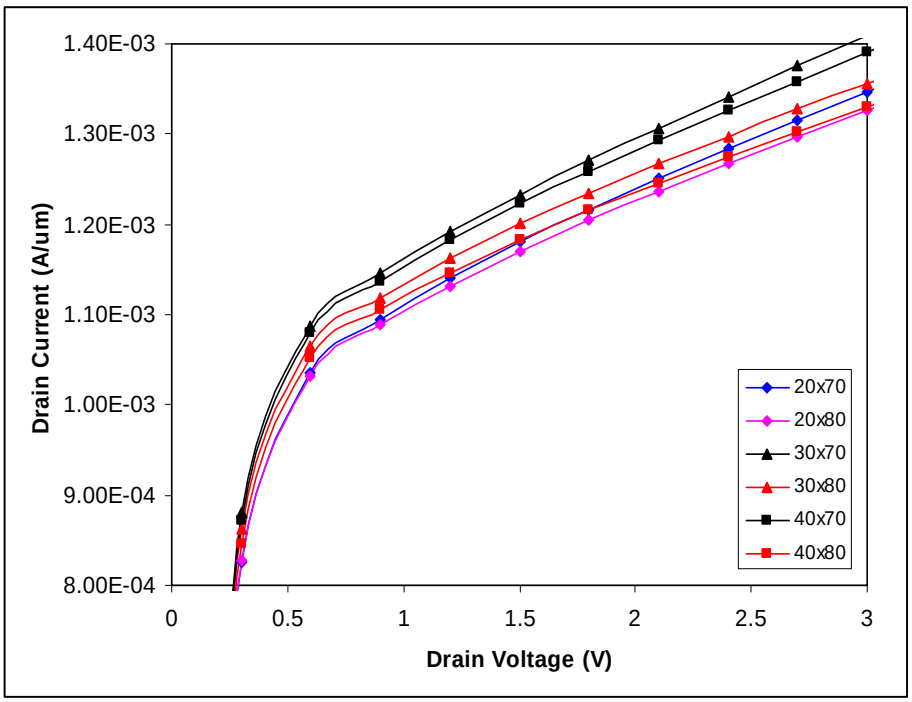

Figure 4: Output Characteristics of 50nm DP-MOSFET with uniform boron doping of 10^{17} cm^{-3} to 10^{19} cm^{-3}.

CONCLUSIONS

The analysis of DP scaled structure from a 50nm DP-MOSFET has been successfully done using commercial ATLAS TCAD tools. By employing the inversion layer mobility model from Lombardi combined with SRH (Shockley-Read-Hall Recombination) with fixed carrier lifetimes models; a detailed investigation on the DP-MOSFET performance was successfully done. From the results, the DP structure of 30nm of width and 80nm of height will be considered the best DP structure according to average performances from electrical characteristics analysis. Besides, the DP has suppressed short channel effect (SCE) and the off-state current can be significantly reduced. Therefore, DP concept is good for scaling the MOSFET in nanometer regime for future development of nanoelectronics product.

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