

SHEAR STRESS ANALYSIS OF DIFFERENT STACKED DIE QFN PACKAGE USING FEM

N.N. Bachok, M.Z.M. Talib and I. Abdullah

*Advanced Semiconductor Packaging (ASPAC) Research Laboratory
Universiti Kebangsaan Malaysia
43600 UKM Bangi, Selangor, Malaysia*

ABSTRACT

Package of stacked die QFN nowadays become more popular in semiconductor industry because of its lead less, good electrical performance and its small size. However, it is not an easy task to manufacture a robust stacked die QFN. Usually, die shear test will be conducted with specified condition to test the die strength. Die contains circuit that is significant part of the package. In this paper, Finite Element Method is used to perform the shear stress of the stacked die QFN package. Shear stresses are simulated to determine the die shear strength as to predict the integrity of materials used in stacked die QFN Package. Five different model which include one single die QFN package and other four model of stacked die QFN are developed in this study; they are conventional single die, two layers pyramidal stacked die, over hang stacked die with spacer, three layers and four layers stacked die with spacer. Some components of stress which also includes the shear stress of each package are determined to see the performance of the package. Comparison between few models of stacked die QFN shear stress result and effect of stacking die on the package are analyzed and discussed. Finally, it is suggested that finite element method can be used to simulate the shear stress of different stacked die QFN package.

INTRODUCTION

Semiconductor industry is driving towards miniaturization, multifunctional and high density packages especially for portable electronic devices. The development of IC packaging history showed that it is a competition of miniaturization [1]. The demand of miniaturizing IC packages by customers brought this trend of reducing the weight and size of the package. QFN is one of the type in IC packaging. QFN also known as micro lead frame (MLF), micro lead package (MLP), quad outline non-lead (QON) or small outline non-lead (SON) package. It is type of CSP which is chip scale package [2].

Parallel to the semiconductor establishment, stacked die QFN package has become popular IC package in electronic industry. Technology of stacking multiple die in the package can reduce the total foot print up to 28% [3]. It also can reduce total cost for the low pin count requirement application. Silicon die, lead frame, mold compound, and die attach paste are main components contained in conventional

Corresponding Author: qurrata_nadzmy7@yahoo.com

QFN [4]. These components also exist in stacked die QFN where several die includes in the package.

It is not easy to design stacked die in order to include several dies in a well-accounted layout. Product manufactures are usually concerned on the reliability of the package. Previously, development package cycle includes design-build, test- and redesign type of package. This tradition cycle is no longer relevant and efficient for competitive semiconductor industries which put accent on short time to market. It takes 3 - 4 months to complete the package and test the reliability which also require expensive test equipment and manpower for data collection [5]. The stress results will be very important data for designers in semiconductor packaging to optimize QFN design structures. Currently, there are not so many publications available on reliability modeling of QFN package [6].

It is shown by some previous study that finite element modeling is widely used in semiconductor field. One of them is an analysis tool for solder joint reliability [7]. This study was done to see the transient deformation and fracturing of solder joints subjected to the impact load. Finite element analysis also was used to determine the time dependent solder joint fatigue response of a tape chip scale package under accelerated temperature cycling condition [8]. By using this method, effects on different ball via configuration can be investigated. This tool was chosen because the process of thermal cycling test is time consuming and costly [9]. So by choosing finite element analysis, it can reduce the cost of experiment, development and also the time.



Figure 1: Shear test machine.

In IC packaging test, die shear test is used to determine the integrity of materials and procedures used to attach semiconductor die or surface mounted passive elements to

Corresponding Author: qurrata_nadzmy7@yahoo.com

package headers or substrates. This determination is based on a measure of force applied to the die, the type of resulting force applied to the die, the type of failure resulting from this application of force (if failure occurs) and the visual appearance of the residual die attach media and substrate/header metallization. Figure 1 shows the image of instrument be used in die shear test. Therefore, in this study, finite element method is used to determine how the die stacking structures affect the package robustness. Five different models are developed to determine the stress of the package due to the process of manufacturing and the reliability test. Instead of developing five real models to be tested, this finite element method is another way to do the analysis on the robustness of the package.

METHODOLOGY

Finite Element Analysis

In this paper, five different QFN package are modeled. They are one conventional single die model (SD 1+0), two layers pyramidal stacked die (SD 2+ 0), overhang stacked die with spacer (SD 2+1), three layers (SD3+1) and four layers (SD 4+1) pyramidal stacked. Three dimension FEA models are developed in this study to see the die shear stress of each package. Finite element analysis is not a method to determine the actual stress value, but it is quite close to compare the differences between this few models. From previous study, as long as the analysis approach, meshing and the use of material properties are same, a precise evaluation can be acquired.

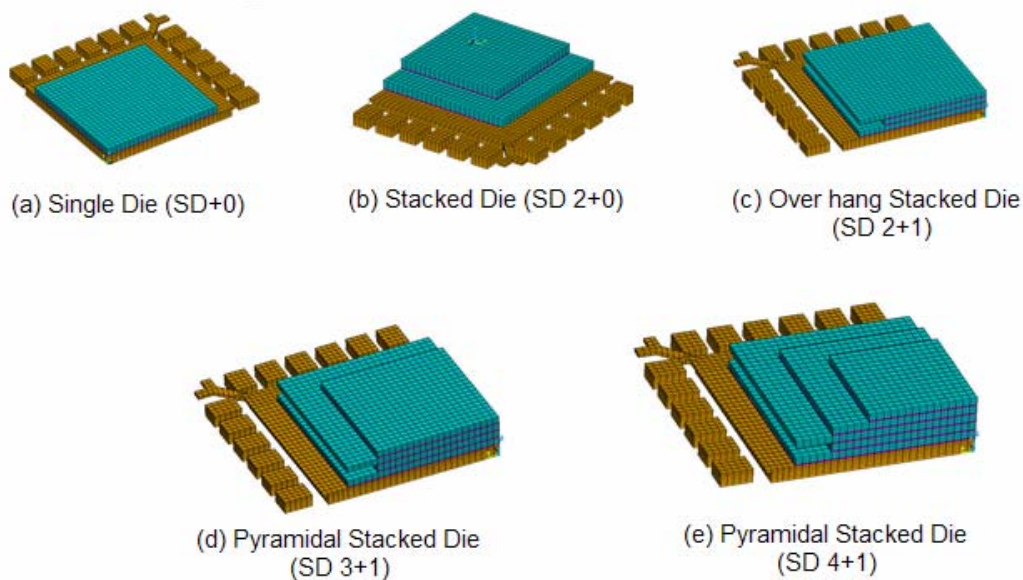


Figure 2: Five Stacked Die QFN Configuration Model.

For this simulation, the unit package size used is $7 \times 7 \times 0.85 \text{ mm}^3$. This package has

Corresponding Author: qurrata_nadzmy7@yahoo.com

48 leads at the bottom of the package and used three different die sizes for five configurations. The die sizes are 5 x 5 mm, 4 x 4 mm and 3 x 3 mm with the thickness of 0.15mm for (SD 1+0) and (SD 2+0) model, and 0.10mm for the other model. As an alternative to build a complete geometry model, it is acceptable to build only quarter model. Only quarter model of each packages were built to represent the whole package as it has a symmetrical boundary condition imposed. Five configurations of stacked die QFN are shown in Figure 3. The figures only show three main components inside the stacked die QFN package that are lead frame, dies and die attach. Mold compound elements are detached for better revelation.

Loading Definition in Finite Element Analysis

Analytically, quarter model packages were built to represent the whole packages stress. It is due to the symmetrical boundary condition. One of this simulation assumptions is the base of leadframe will fix and attach at PCB. Therefore, the degree of freedom for leadframe basement is zero. The thermal loading use in this simulation is 260°C. This value refers to IPC/ JEDEC J-STD-020C. Table 1 below shows package classification reflow temperatures for Pb-Free package. All five models package thickness in this study is 0.85 mm and classified as less than 1.6mm. From this standard, a Pb-Free component shall be capable of being reworked at 260°C within eight hours of removal from dry storage or bake. To verify the capability for a component classified at temperature below 260°C, a sample of the size shall be soaked using some conditions and reflowed at classification of 260°C. All devices must have damage less than rated at MSL Level.

Table 1: Pb-Free –Package Classification Reflow Temperature.

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 +0 °C *	260 +0 °C *	260 +0 °C *
1.6 mm - 2.5 mm	260 +0 °C *	250 +0 °C *	245 +0 °C *
≥2.5 mm	250 +0 °C *	245 +0 °C *	245 +0 °C *

* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0°C) at the rated MSL level.

RESULTS OF THE DIE STRESS ANALYSIS

Result of stress for each model will be acquired after the simulation software solves the solution. The stress value obtained by the simulation will represent the structural reliability of the model. Hence, this stress value will be used to compare all the five configuration of stacked die QFN package model. There are many different stress value obtained by the simulation; but in this study only six

Corresponding Author: qurrata_nadzmy7@yahoo.com

significant die stresses will be compared for each model. The stresses are *yz* and *xz* shear stress, *x*, *y* and *z* component stress, and the 1st principal stress.

Shear Stress

Table 2 and Figure 3 show the XZ and YZ shear stress result for each configuration. It is shown that both the YZ and XZ shear stress of the die give the same result. This significant result shows that each model has same value both of their shear stress. This happened because the die is square. The die length and width are same. The maximum YZ and XZ shear stress area also at the same location. Figure 4 indicated the YZ shear stress result for SD2+0 and SD2+1. The red circle shows the maximum die shear stress location. SD2+0 models have the largest shear stress and SD2+1 has the smallest shear stress. The results showed that the stress value increase with the number of dies in the package. The double stacked die showed increment up to 2.4% compared to the single die model. However, by adding a spacer to the model, it will reduce the shear stress value. The stress value was reduced by 11% by adding a spacer to model (SD 2+1) compared with model (SD2+0). The increment of the fourth model compared with the third model, and the fifth model with fourth model, both were only 0.15%.

Table 2: YZ Shear Stress and XZ Shear Stress Result.

Model\Shear Stress	YZ Shear Stress	XZ Shear Stress
SD 1+0	0.730e7	0.730e7
SD 2+0	0.751e7	0.751e7
SD 2+1	0.672e7	0.672e7
SD 3+1	0.673e7	0.673e7
SD 4+1	0.674e7	0.674e7

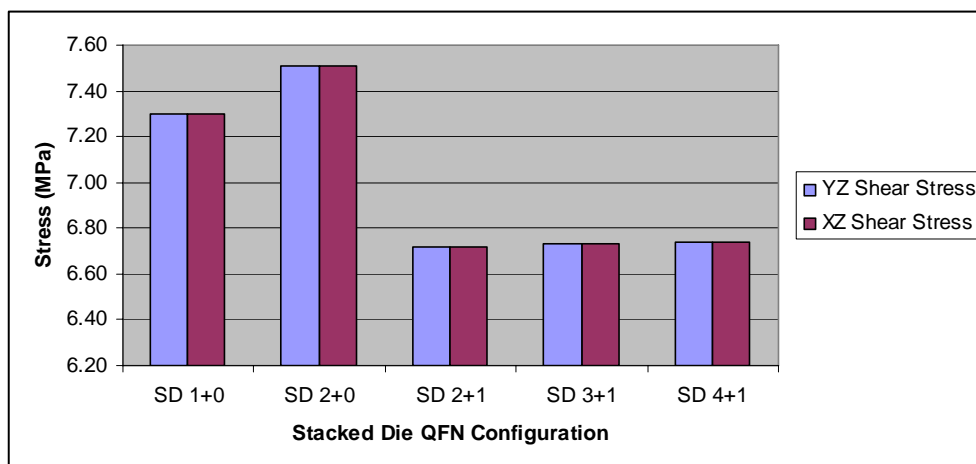


Figure 3: Shear stress result for five stacked die QFN model.

Table 3 and Figure 5 below show result of component stress for five configuration of stacked die. The crack at the die is caused by the tensile stress. In a tension test, the fracture occurs when the normal stress reaches the ultimate stress. The depth of the crack depends on the stress level in the package. Hence, stress in vertical direction can show the possibility of delamination between two materials. Figure 5 shows the horizontal and vertical direction stress for the five models. All stacked die with spacer model has the highest die stress at reflowed temperature. They higher than the single die model for 22% at that temperature. Figure 6 shows vertical direction stress for single die model and stacked die with spacer (SD 4+1) model. In Figure 4(a) some elements of the first and second and upper layer are removed to get a better visualization. The maximum z- direction stress location occurs at the edge of the die.

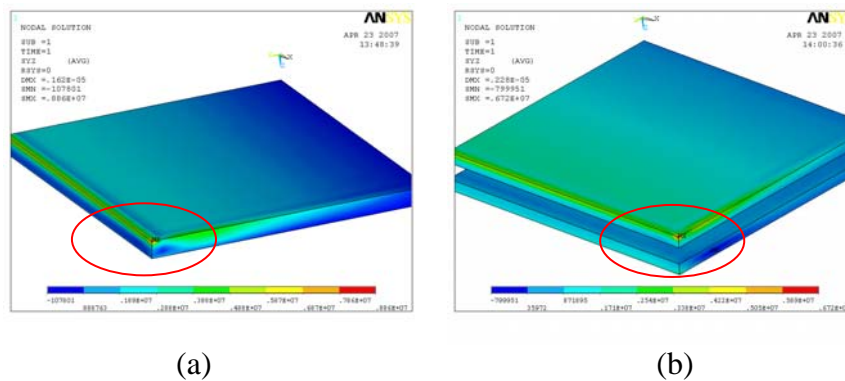


Figure 4: (a) YZ shear stress for model SD2+0, (b) YZ shear stress for model SD2+1.

Table 3: Component Stress Result.

Model\Component stress	X Stress	Y Stress	Z Stress
SD 1+0	599073	606821	0.153e8
SD 2+0	585022	613813	0.166e8
SD 2+1	0.708e7	0.706e7	0.187e8
SD 3+1	0.687e7	0.685e7	0.187e8
SD 4+1	0.689e7	0.688e7	0.187e8

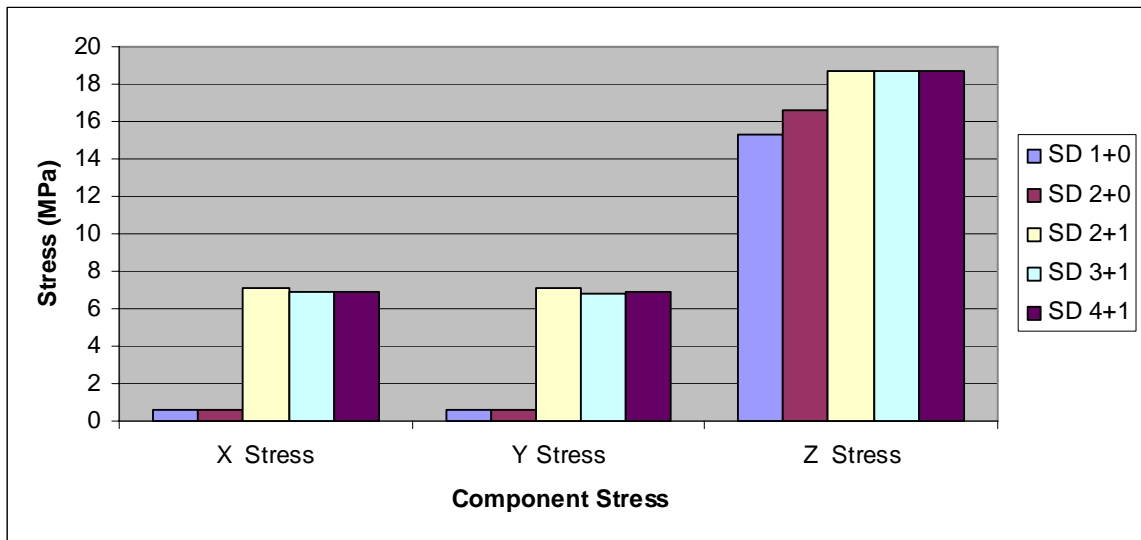


Figure 5: Component Stress Result for five models.

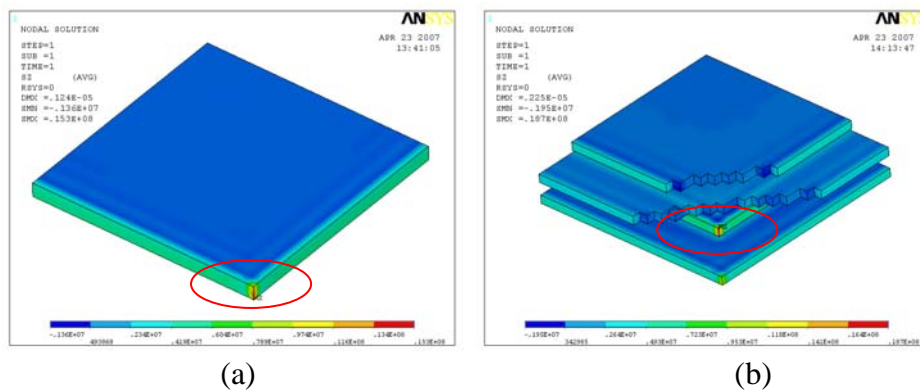


Figure 6: Highest vertical direction stress location for (a) single die (SD 1+0) and (b) stacked die with spacer (SD 4+1).

Table 4: Results of the 1st Principal Stress.

Model	1 st Principal Stress
SD 1+0	0.181e8
SD 2+0	0.183e8
SD 2+1	0.190e8
SD 3+1	0.190e8
SD 4+1	0.190e8

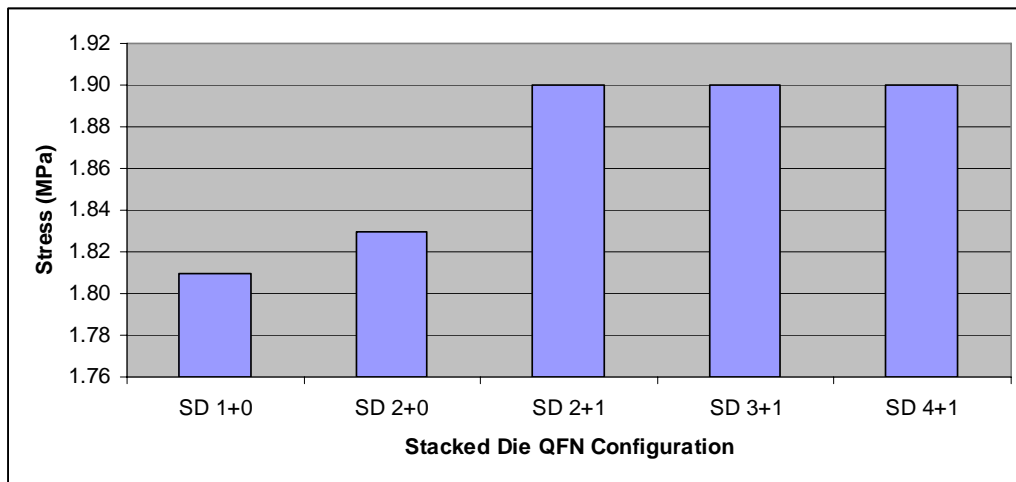


Figure 7: 1st Principal Stress Graph.

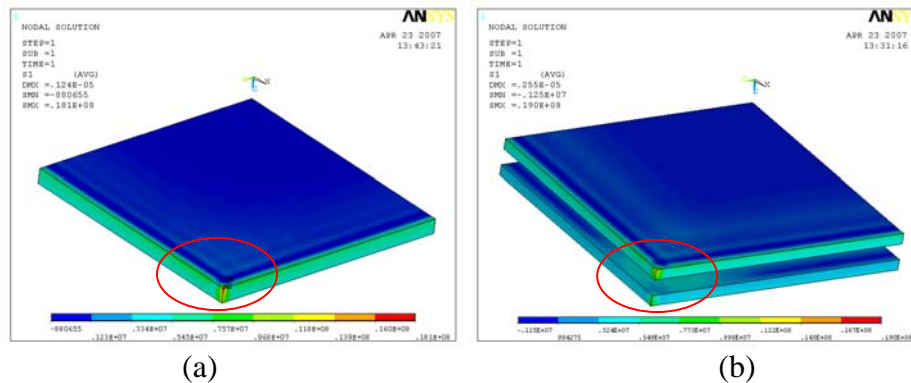


Figure 8: Highest die first principal stress location at the edge of the die for two models: (a) (SD 1+0), (b) (SD 4+1).

1st Principle Stress

Another significant stress in die is 1st principal stress, as shown as the graph in Figure 7. Principal stress theory provides satisfactory results for brittle material like die. A brittle material will fail when the maximum principal stress in the material reaches a limiting value that is equal to the ultimate normal stress the material can sustain when it is subjected to simple tension. From the result below, the highest die maximum principal different model (SD 2+1), (SD 3+1) and (SD 4+1) that is 1.9 MPa. But, the different of the value for stacked die model with spacer and single die model is only about 5%, and still under the acceptable limit. This result also shows that by adding a spacer to the stacked die package will stop the increment of the 1st principal stress value that can perform almost like a single die package. Figure 8 shows the highest die first principal stress location for single die model and stacked die (SD 4+1) model at reflow temperature, 260°C. Both results show the location of highest 1st principal stress is at the edge of the die. This location is the area where the die crack possible happened. Since both of the value

Corresponding Author: qurrata_nadzmy7@yahoo.com

of stress is still less than 0.4 GPa, it is not considered as having high risk for die crack.

CONCLUSION

FEM was performed to analyze shear stress of different stacked die QFN package. Besides, FEM also can be used to analyze other significant stress on the die. The die stress was analyzed to determine the location of crack area and the possibility of crack occurrence. Five different die stacking structure 3-D quarter models were created to determine the thermally induced stress on the package.

From the simulation result, it is shown that, by adding a spacer to the stacked die package, the shear stress was 11% lower than stacked die package without spacer. The number of shear stress did not increase with the number of die stacking with a spacer in the package. But, it did not so without spacer package model. The shear stress increased from single die to the double die for temperature of 260°C. The trend of vertical direction stress and first principal stress seemed to be identical. Stacking double die in a package increased both the Z stress and first principal stress from single die package. Using a spacer did not reduce the stress, but stacking dies with spacer will stop the increment of the stress even the number of die is increased. The difference of first principal stress value between single die and stacked die with spacer (SD 4+1) is only 5%.

Finally, it is suggested that the multiple stacked dies package could perform better in terms of its robustness. The FEM can be used to determine how the trend of stress occurs at the dies and also other main components in the IC package.

REFERENCES

- [1]. I. Anjoh, A. Nishimura and S. Eguchi, (1998); Advanced IC Packaging for the Future Applications. *IEEE Transactions on Electronic Devices* **45**: 743-752.
- [2]. T.Y. Tee, H.S Ng, and J.L. Diot, (2002); Comprehensive Design Analysis of QFN and Power QFN Packages for Enhanced Board Level Solder Joint Reliability. *2002 Electronic Components and Technology Conference*, pp. 985-991.
- [3]. T.Y. Tee, M. Lim, H.S. Ng, X. Baraton, D. Kaire and Z. Zhaowei, (2002); Design Analysis of Solder Joint Reliability for Stacked Die Mixed Flip Chip and Wirebond BGA. *2002 Electronic Components and Technology Conference*, 391-397.
- [4]. C.C. Ng, G. Govindasamy, and T.M.Y.S. Tuan Ya, (2005); Warpage Analysis and Thermo-Mechanical Stress Modeling of QFN Molded Strip. *5th ASEAN ANSYS User Conference 2005*, 234- 241.
- [5]. T.Y. Tee, H.S. Ng, J.E. Luan, X. Zhang, K.Y. Goh, A.M. Grech & R. Duca, (2005); 4-Dimensional Design Analysis and Optimization of

- System-in-Package. 2005 *Electronics Packaging Technology Conferencem*, 321-327.
- [6]. T.Y. Tee and Z.W. Zhong,, (2003); integrated vapor pressure, hygroswelling, and thermo-mechanical stress modeling of QFN package during reflow with interfacial fracture mechanics analysis. *Microelectronics Reliability* **44**:105-114.
- [7]. C.L. Yeh and Y.S. Lai, (2004); Transient Simulation of Solder Joint Fracturing Under Impact Test. *2004 Electronics Packaging Technology Conference*, 689-694.
- [8]. B.A. Zahn, (2002); Impact of Ball Via Configurations on Solder Joint Reliability in Tape Based Chip Scale Packages. *2002 Electronics Components and Technology Conference*., 1475-1483.
- [9]. C.C. Ng and G. Govindasamy, (2005); Effect of Die Stacking Structures on QFN Package Robustness. *Semicon ® Singapore 2005*, 1-6.