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FAILURE ANALYSIS OF POWER MOS DEVICE FROM THE BACKSIDE OF THE DIE

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ABSTRACT

Backside analysis has been developed as a useful tool for failure determination for quite some time. This method of analysis, used for debug and fault isolation required a limitless stretch of the imagination and creative solutions. The procedures used to gain access to the back of the target die for backside Photoemission Microscopy have created many unique and challenging solution of their own. With the speed of change, advancement and developments within the power semiconductor technology, multi layer metallization and shrink processes make traditional front or top side analysis technique more difficult and in most cases impossible. Technological advancement results in utilization of backside analysis technique to become an important tool for debug and fault isolation.

INTRODUCTION

Localization of current leakage fault in modern ICs is a major challenge in failure analysis [2]. There are several techniques such as Liquid Crystal Thermography and Emission Microscopy that can be used to isolate this issue. However, trend as the appearance of power semiconductor technologies has driven alternative approaches from the backside of the die rather than traditional frontside failure analysis techniques which are unable to localize fault obscured by several metal layers. Thus, the development of backside analysis for failure determination is very essential due to the thick power metal layer. To enable successful failure analysis for this die type, a backside failure analysis technique as shown in figure 1 was developed which contain failure verification, failure localization using backside emission to isolate the possible failure and finally, FIB cut was done to reveal the root cause of failure.

Failure Characteristics

The threshold voltage, V_{th} shift of the devices was confirmed in the lab. The device electrical parameter extraction is composed of two experiments, the device I_d-V_d characteristics and I_d-V_g characteristics. Afterwards, the parameters are extracted using the experimental data. The I_d-V_d characteristics are measured by applying a

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staircase sweep voltage to the drain (V_d) of the devices and monitoring the drain current. A constant voltage is applied to the gate (V_g) during each sweep, and a group of I_d-V_d data curves can be acquired by varying the gate voltage between sweeps. The I_d-V_g characteristics are measured by applying staircase sweep voltage to the gate (V_g) of the devices and monitoring the drain current. A constant voltage is applied to the drain (V_d) during each sweep, and a group of I_d-V_g data curves can be acquired by varying the gate voltage between sweeps. A bias voltage can also be applied to the substrate contact, (V_b) but to get better extraction results, it is recommend that the bias voltages be set to zero, or at least remain the same in both experiments. The source is grounded in both experiments. Analysis was done using Semiconductor Parameter Analyzer to bench verify and also to further analyze the IV characteristic. Figure 2 and 3 showed I_{dss} high leakage characteristic and V_{th} drift for device 1 undergoing temperature cycling (TC) failed, while Figure 4 showed device 2 undergoing pressure cooker test (PCT) failed V_{th} drift.

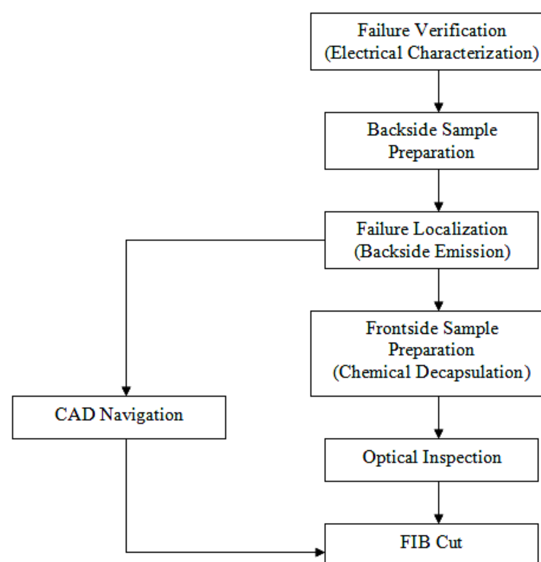

Figure 1: Backside failure analysis for power MOS device.

Backside Sample Preparation

Infrared radiation can be transmitted through silicon substrate material. The difficulty in this process lies within the ability of the silicon material to absorb the IR emissions. The amount of photons that are passed through the silicon material with sufficient infrared intensity for detection significantly depends on silicon substrate thickness, doping density, backside planarity and emission light wavelength. For a specific doped concentration level of silicon material, a thinner substrate has a higher photon transmission rate. For the same thickness of Silicon substrate, a higher doping concentration has a much lower transmission rate [3]. Therefore for power semiconductor device which is heavily doped, thinning of the backside Si substrate to an acceptable thickness of approximately 100 μm is necessary.

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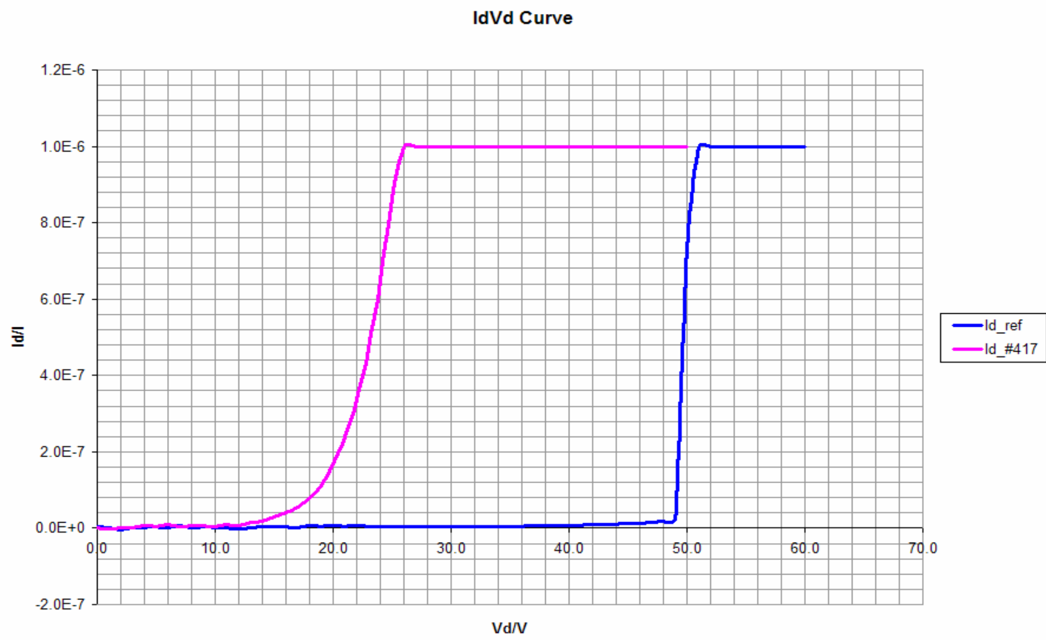

Figure 2: Failed device 1 undergoing TC shows I_{dss} high leakage.

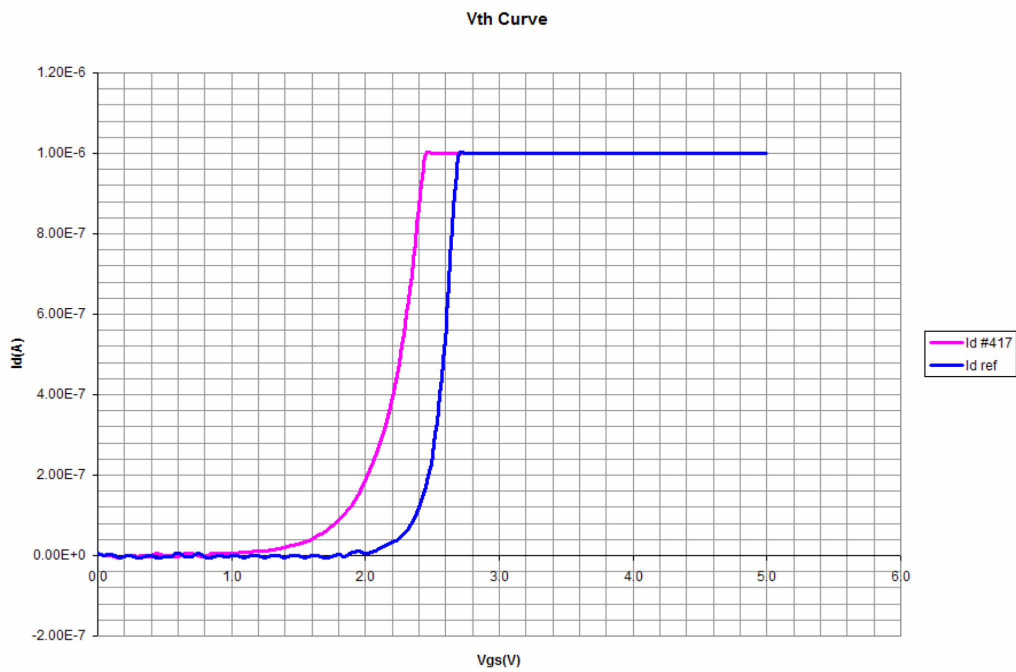

Figure 3: Failed device 1 undergoing PCT shows V_{th} drift.

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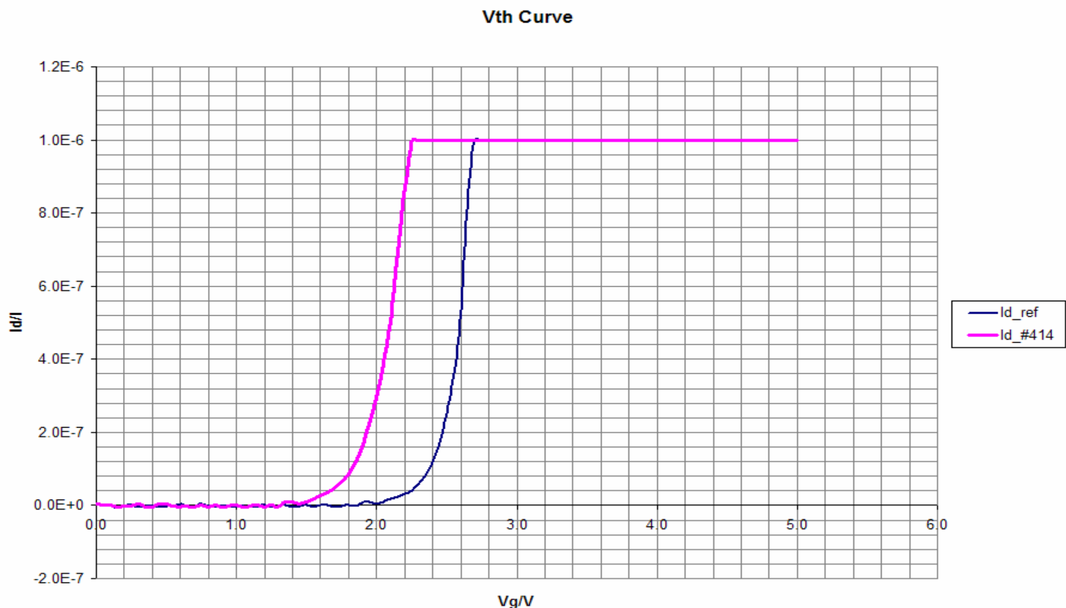

Figure 4: Failed device 2 undergoing PCT shows V_{th} drift.

Mechanical thinning from the back metallization to Si substrate was done using precise Automated Selected Area Polisher. The initial milling of the Si die was done with a diamond milling head with lubricant oil thinning down to 115 µm. Subsequently, sample was pre-polished with a tip using 6 µm diamond slurry mixed with lubricant oil for 20 minutes. Follow by a second pre-polish with finer diamond slurry of 3 µm for another 20 minutes. Final polish was done using tip with Colloidal Silica for 15 minutes and final die thickness is approximately 100 µm.

Electrical Defect Localization Using Photoemission Microcopy

In MOSFETs, when the drain or source is connected to the substrate, any voltage applied to the substrate, and to the gate will drop across the gate oxide. In n-channel devices, an inversion layer of electrons will form at the oxide/silicon interface, creating localized electron trapping. Electrons in the silicon within this region are raised above their ground state and conduct from the silicon into the oxide via Fowler- Nordheim tunneling. Then these already energetic electrons are boosted to higher states by the electric field across the gate oxide. Ultimately, in the polysilicon layer above the gate, these electrons may combine with holes or create new electron-hole pairs. As the electrons and holes combine, they too emit photons.

In another scenario, when deep submicron MOSFET is biased to pinch-off means no carriers in the channel, any additional voltage applied between the gate and the drain results in an intense electric field that generates a continuous hot-carrier current between the gate and the substrate. Still higher bias voltages can result in collisions of high-energy hot electrons which may create more electron-hole pairs. In n-channel devices, these new electrons are swept to the drain and the resulting electric

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field forces the holes to move to the source and substrate. The holes that find their way to the source then can forward-bias the source-substrate junction, creating additional electron-hole pair generation.

Because of the transparency of silicon in the near IR it is possible to detect failures from backside of the devices [4]. Photon emission is typically a result of direct recombination of electron-hole pairs thus defects with leakage profile will enhance further the recombination process. Emission microscopy is well known technique that has only been recently improved to be applied from backside [1][5]. Backside emission analysis revealed a localized emission spots in both ICs devices as shown in Figure 5 and 6. Backside emission was performed using the Photoemission Microscopy System which incorporates an emission microscope and NIR laser scanning microscope. So, emission was done using frontside illuminated C-CCD camera while for imaging, an infrared light is used to illuminate the circuit through the silicon substrate. Then, the circuit is observed with C-CCD camera through a NIR filter. A subsequent overlay with x-ray image confirmed that the spot was located at the bond pad as shown in Figure 7 and 8.

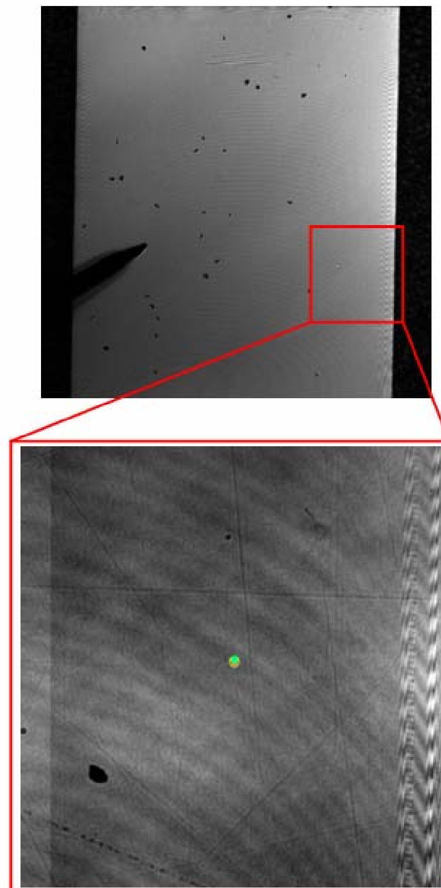

Figure 5: Localized emission spot on device 1.

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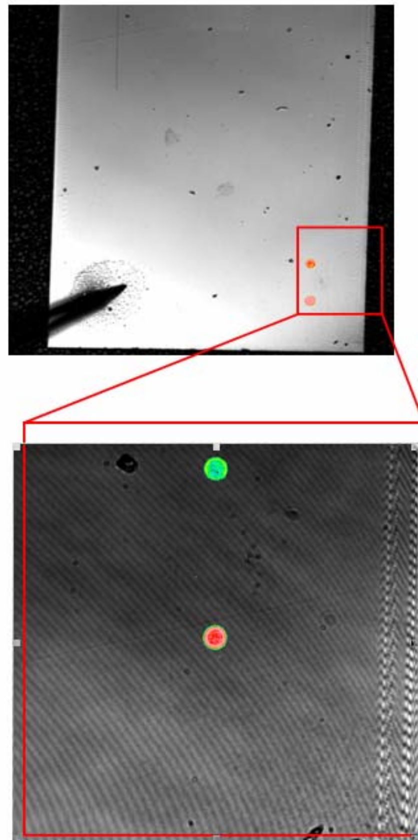

Figure 6: Localized emission spot on device 2.

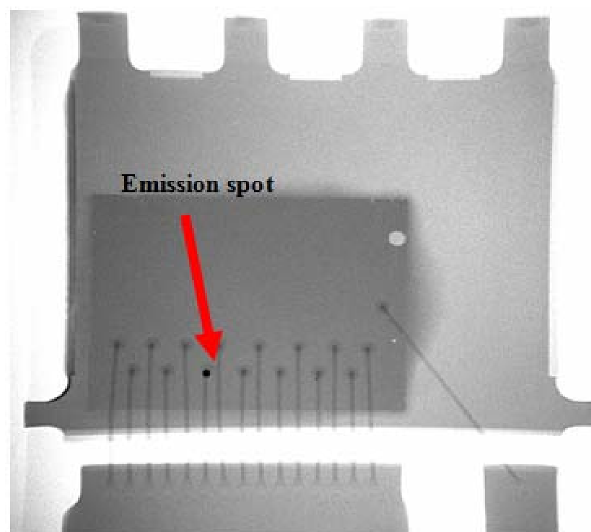

Figure 7: Overlay of the emission microscope image and x-ray image of device 1.

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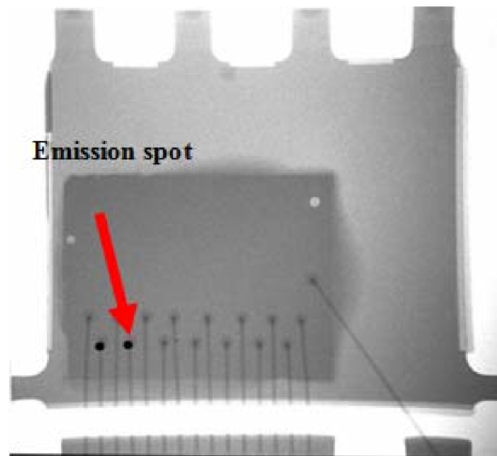

Figure 8: Overlay of the emission image with an X-ray image of device 2.

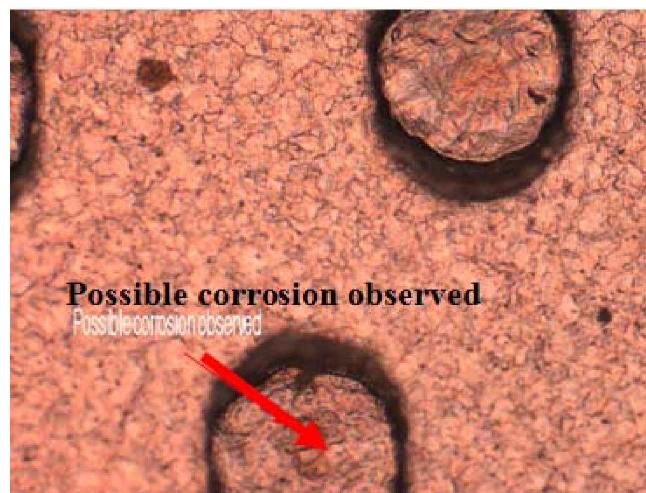

Figure 9: Possible corrosion region.

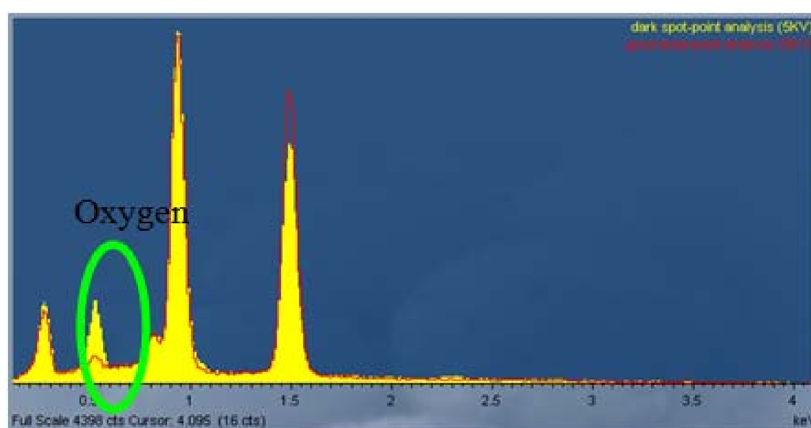

Figure 10: Elemental analysis on suspected corrosion region.

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Chemical Decapsulation

New generation mold compounds and packaging are the challenge to the traditional methods of decapsulation of IC devices. In this technique, fuming nitric acid is used to dissolve the mold compounds. This fuming acid is a very strong oxidizing agent and very vigorously attack Copper (Cu) and Silver (Ag) element. HNO_3 acid should be mixed with 10% concentrated sulphuric acid to avoid any damage to Cu or Ag material. It is also very important to keep the exposure of the reactive acid in a very short period to avoid accidental over-etching of the device. This process is repeated several times until the mold compound is sufficiently exposed. Finally, acid residues are removed by rinsing with de-ionized water and acetone.

Optical Inspection

Optical inspection after decapsulation and removal of ball bond for both IC devices revealed possible corrosion region as shown in Figure 9 and was conformed upon EDX analysis as shown in Figure 10. Higher oxygen element was found at the suspected corrosion region (dark spot) during elemental analysis.

Post Analysis Using FIB

Beside the emission microscope, various systems such as SEM, FIB and TEM are used for failure analysis. As each analysis is done separately, it takes usually very long time to get exact conclusion. It is getting indispensable now to exchange common database through CAD Navigation System as it is more benefit to save the searching time of the failure point in other analysis system by exchanging the coordinate information of the failure point found by emission microscope through navigation system. For this case study, the layout data is needed to assist during FIB cut process. FIB cut was performed on the emission spot region for both IC devices respectively. FIB image as shown in Figure 11 revealed crack of the power metal at the emission spot, while Figure 12, for both emission spot revealed possible path susceptible to ionic contamination via metal grain boundaries. No crack was observed for this IC device.

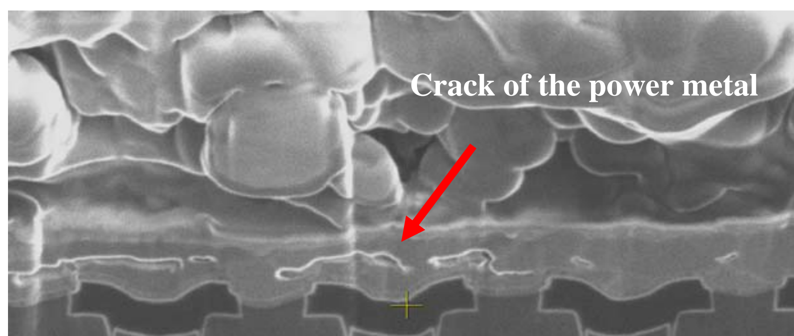

Figure 11: FIB Cross sectioning on device 1 revealed crack of the power metal.

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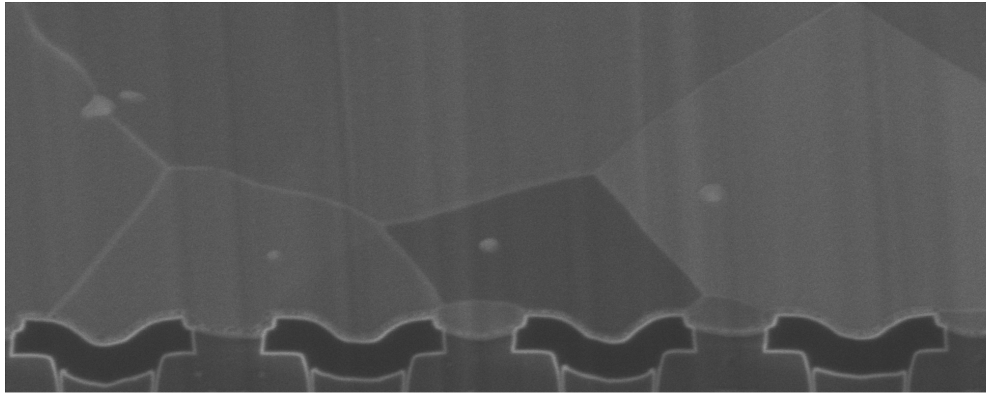

Figure 12: FIB Cross sectioning on device 2 revealed possible paths to ion contamination failure mechanism.

RESULTS AND DISCUSSION

Result basically shows the crack of the power metal most likely is the path which is suspected for mobile ion contamination diffusion to the gate oxide thus correlates with V_{th} drift failure mechanism. Ionic contamination in semiconductor devices is one of the common failure mechanisms. As a result of mobile ion contamination, IC devices can suffer changes in the carrier concentration resulting in threshold voltage shifts, an increase in leakage current and gain reduction.

CONCLUSION

The development of failure analysis technique from the backside proved to be vital for the power MOS device technology whereby it is much easier to get access to the die from the back rather than the front side due to the thick power metal.

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